

# Chapter 1

## Introduction

In this chapter, compact models for the metal-oxide-semiconductor (MOS) transistor are briefly introduced and their evolution since the late 1960s is summarized.

### 1.1 MOS integrated circuits

During the initial years, from the early 1960s until the late 1970s, the design of integrated circuits (IC) was the domain of circuit designers working within semiconductor companies. This paradigm started to change in the early 1980s, after the introduction of the text “Introduction to VLSI Systems”, by Carver Mead and Lynn Conway [1]. The Mead-Conway text was written to fill a gap in the literature and to introduce electrical engineering and computer science students to integrated system architecture and design. Instrumental in the wide diffusion of the IC design capabilities were the multiproject chip initiatives which began in the 1980s. The access to fast prototyping of chips has allowed engineers other than those working within semiconductor companies to design VLSI chips.

During the 1970s, nMOS was the dominant technology for highly complex digital circuits. In the early 1980s, CMOS became the technology of choice for general-purpose integrated circuit applications [2]. Advantages of CMOS technology include low static power consumption, simple laws of scalability, and stability of operation [2]. Finally, the CMOS technology has proven to be useful not only for digital circuits but also for analog and RF circuits; as a result, many chips

today are complete systems thanks to the flexibility and scalability of the CMOS technology.

As a consequence of the explosive growth of the IC business, including fab and fabless companies, a large number of circuit designers work without having regular interaction with the process and manufacturing engineers. The designers rely on the simulation of their design before building a prototype. To simulate a circuit, simulators make use of element models, which provide a mathematical description of the element behavior in the circuit. The compact MOSFET models provide most of the designers with the essential information concerning electrical properties of the components associated with the manufacturing process of the chip.

## **1.2 Compact MOSFET models for circuit analysis and design**

Computer aided design (CAD) tools are essential elements for circuit design. The productivity of circuit designers is intimately associated with the efficiency of the available arsenal of CAD tools. One of the most useful IC design tools is the circuit simulator, which allows users to enhance the understanding of a circuit and some fine details of its operation. The judicious use of electrical simulators allows the quick evaluation of the circuit performance without the burden of a costly integrated prototype. One must bear in mind, however, that the accuracy of the results provided by the simulator depends on the quality of the circuit element models. Thus, MOSFET models, which serve as the critical communication vehicle between circuit designers and silicon foundries [3], play a crucial role in chip design productivity.

At this point, we differentiate between two categories of device models [4], [5], namely numerical device simulation models and compact models. Numerical device simulators are used to study the device physics and to predict the electrical, optical, and thermal behavior of a device. Numerical device simulators solve a set of (partial differential) equations associated with the physics involved in device operation; their requirements of intensive computation and huge amounts of memory prevent them from being used for circuit simulation. On the

other hand, compact models or equivalent circuit models describe the terminal properties of the device by means of a simplified set of equations or by an equivalent circuit model. Of course, device simulators can be very helpful in the task of determining the equivalent circuit of a device.

This book deals with compact models of the MOS transistor for circuit analysis and design. The purpose of a compact model is to obtain simple, fast, and accurate representations of the device behavior. Compact transistor models are needed to evaluate the performance of integrated circuits containing a large quantity of transistors, sometimes several thousands. MOSFET compact models fall into three categories: (1) Physical models, based on device physics, (2) Table lookup models, in the form of tables containing device data for different bias points, and (3) Empirical models, which represent the device characteristics through equations that fit data. Physical models take considerable time to develop but once they become mature, their advantages are significant: parameters have physical meaning, effects of device geometry, technological parameters, and temperature can be accounted for, statistical modeling can be applied to predict ranges of expected performance [6] and, in many cases, the model can be applied to different generation technologies by simply changing parameters. Throughout this book, we will mainly deal with physical models. We strongly believe that circuit designers who have a background in the physical phenomena behind transistor operation are more capable of quickly analyzing a circuit topology, understanding its limitations, and more easily interpreting simulation results, besides being more ingenious and creative in their designs.

### **1.3 A brief history of compact MOS transistor models**

In the late 1960s and early 1970s, simulation programs aimed at analyzing nonlinear circuits began to be developed. The purpose of this development was mainly to test new circuits made available by the nascent field of integrated circuits. SPICE (Simulation Program with Integrated Circuit Emphasis), released in 1972, is the most tangible result

of the effort in developing simulation programs at UC Berkeley [7]. Since its beginning, SPICE or one of its many derivatives has been an invaluable resource in evaluating IC performance prior to its integration [8].

Essential to SPICE-like simulators are the element models, and, in particular, a compact model for the MOS transistor.

The first MOSFET model for the SPICE circuit simulator, the Level 1 model, often called Shichman-Hodges model [9], is a simplified first-order model suitable for long-channel transistors only. Level 1 describes the current dependence on voltages for gate voltages greater than the threshold voltage; the sub-threshold current is assumed to be zero. In addition, the terminal capacitances, which are described by the Meyer model [10], are not charge-conserving.

The Level 2 model addresses second-order effects associated with small-geometry devices. Unlike in Level 1, the sub-threshold current is not equal to zero. The capacitive model can be either the Meyer model [10] or the Ward-Dutton model [11], the latter conserving charges. Level 2 is computationally very complex and convergence problems are often encountered [5], [12]. The many drawbacks of Level 2 are extensively commented on in [3].

The Level 3 model is a semi-empirical model developed to address the shortcomings of Level 2. It runs faster than Level 2 and convergence problems are seldom encountered. The capacitive model of Level 3 is the Ward-Dutton model. Failure to properly model the sub-threshold current and the output conductance are two of the major drawbacks of Level 3.

The rapid evolution of the MOS technology in the 1980s showed that the Level 1, 2, and 3 models were clearly not appropriate to simulate efficiently circuits with a large number of ever-smaller transistors. A different modeling philosophy to that employed for first generation models was then adopted. BSIM (Berkeley Short-Channel IGFET Model) [13] inaugurated a second generation of MOS transistor modeling, which put less effort into developing physical models but instead concentrated on mathematics for faster and more robust circuit simulation [3]. Convergence problems and negative output conductance were some of the problems that inhibited the use of BSIM for analog designs. Two later developments, BSIM2 and HSPICE Level 28, with

comprehensive modifications of BSIM, made second-generation simulators suitable for analog IC design [12]. The most important shortcomings of second-generation models are their empirical and complex implementation, which incorporates several parameters without clear physical meanings [12].

BSIM3 and its extension BSIM4, along with MOS Model 9, brought into the public domain by Philips, began the third-generation approach [12] of the 1990s, which reintroduced the physical basis into the models. The use of smoothing functions in third-generation models provides continuous and smooth behavior of device characteristics across all the operating regions. Even though it follows the general trend of third-generation models, the EKV model [14] is a fully symmetrical model which uses the bulk voltage as the reference.

The first, second, and third-generation models previously mentioned were the most used for integrated circuit design over the 30-year period, from 1970 to 2000. In these models, the current and charges are approximated by explicit functions of the terminal voltages. The approximate solutions are obtained by interpolating models that are only valid in particular regions of operation. This leads to inaccuracy between operating regions and, thus, inaccuracy in the simulation of circuits where transistors operate between these regions [15]. A considerable effort in academia and companies has been made in the last few years to provide the design community with better compact models that can lead to more accurate simulation results. The development of more accurate models, together with the physics behind them, and a review of some landmark papers concerning compact MOSFET models will be the main subjects of this textbook.

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