

PREFACE

N. RANGANATHAN

*Center for Microelectronics Research
Department of Computer Science and Engineering
University of South Florida, Tampa, FL 33620, USA*

Many problems in pattern recognition, artificial intelligence, image processing and computer vision have applications in automatic parts inspection and assembly, robotic vision and control, image registration, geographic and topographic map matching, navigational guidance, target recognition, character recognition, chromosome classification, interpretation of medical images, scene analysis etc. Pattern recognition often involves matching patterns of different shapes, sizes and representations. The task of pattern matching could be complex and computationally intensive depending upon the application and the procedure used. Similarly, in the fields of image processing and computer vision, the performance of sequential computers has been found to be quite inadequate since most applications require processing in real time. A 1024×1024 image frame with 256 gray levels requires 8 M pixels for storage and most applications require the storage and processing of multiple frames at very high speeds. Multimedia and video applications require frame rates of 50 to 80 frames per second. Thus, the throughput requirements of these applications could run into giga operations per second. Such tasks often perform a large number of repetitive computations on different data sets, make use of regular and local operations, are modular, and have a fair amount of inherent parallelism. With the rapid advances in VLSI technology and parallel processing, the design of high performance hardware for such computationally intensive tasks has become an attractive solution in real-time applications.

VLSI technology has progressed rapidly in the past decade leading to high packaging densities, decrease in gate delays, decreasing fabrication costs, powerful CAD design automation tools, and reliable and fault-tolerant design strategies. The attributes of parallelism, concurrency, pipelining, modularity and regularity have become standard features of hardware designs. Thus, the VLSI microelectronics technology has led to the design of massively parallel array processors and parallel computers towards meeting the challenge of high performance computing applications.

In this book, a set of twelve papers are included which cover a wide range of problems in the areas of VLSI and pattern computing. The first paper is an important contribution by M. C. Herbordt and C. C. Weems who present a software system architecture for use in evaluating massively parallel array architectures for spatially mapped applications. They have addressed the issues of flexibility of design space, simulation efficiency, programmability of test suite, fairness of evaluation and accuracy. The next paper by S. M. Bhandarkar, H. R. Arabnia and J. W. Smith

describe a reconfigurable architecture for image processing and computer vision based on a multi-ring network topology. They describe parallel algorithms for FFT and the Hough transform to illustrate the efficiency of their proposed architecture. Two papers are contributed by N. Venkateswaran *et al.* on the design of array processors for applications in image processing and signal processing. They have developed design methodologies for efficiently constructing large VLSI array processors in a systematic manner optimizing on cost and performance.

In the next paper, A. K. Bhattacharya and S. S. Haider describe the design of a VLSI chip for computing the Inverse Discrete Cosine Transform (IDCT), a project undertaken at the AT&T Bell Laboratories. The IDCT computation is used for image compression in multimedia systems, HDTV and digital TV complying with standards such as JPEG and MPEG. In the sixth paper, M. Albanesi and M. Ferretti describe a VLSI chip-set for computing the Generalized Hough Transform, an important function used in object recognition. An interesting contribution comes from T. Acharya and A. Mukherjee as the seventh paper which describes a VLSI chip architecture for real-time lossless image compression. R. Sastry and N. Ranganathan describe the design and implementation of a VLSI chip for polygon matching and recognition. The recognition procedure is based on a dynamic programming scheme employed for string matching and is based on the concepts proposed by T. Glauser and H. Bunke.

The ninth paper by H. Senoussi and A. Saoudi describe quadtree algorithms for template matching on mesh connected computer. In the next paper, K. L. Chung proposes a parallel algorithm for finding all occurrences of a pattern within a given text, an important problem in computer vision, pattern recognition and image processing. A VLSI architecture for implementation of fuzzy expert systems is proposed in the eleventh paper by V. Catania and G. Ascia. The final paper by I. Ghosh and B. Majumdar describes a VLSI chip for image rotation in real-time.

This book covers parallel algorithms and architectures and VLSI chips for a range of problems in image processing, computer vision, pattern recognition and artificial intelligence. The specific problems addressed include vision and image processing tasks, Fast Fourier Transform, Hough Transform, Discrete Cosine Transform, image compression, polygon matching, template matching, pattern matching, fuzzy expert systems and image rotation. The collection of papers would give the new reader a good introduction to the state-of-the-art while for an expert, this would serve as a good reference and a source of some new contributions in this field.

I would like to thank all the authors for making significant contributions to this book. It should be noted that this book is a reprint of a special issue of *International Journal of Pattern Recognition and Artificial Intelligence (IJPRAI)*. The task of reviewing papers and making recommendations could be very time-consuming and I would like to express my sincere appreciation to all the referees for reviewing the original as well as the revised manuscripts. The idea of this book came up due to the inspiration and encouragement from Horst Bunke, Editor-in-Chief of IJPRAI and I express my gratitude to him. Also, I thank Barbara Aman, editor and World Scientific Publishing Co. for the prompt publication of this book.