

Broadband and Radio Frequency MOS Technology Amplifiers

9.1.0. Introduction

Rendering an amplifier functional at progressively higher signal frequencies has been an underscored focus of analog circuit research and development activities since the day that DeForest introduced the technical community to his vacuum tube. Propelled by the omnipresent need to communicate, quickly and faithfully, large amounts of information and data in commercial, military, and space system applications, broadbanding interests continue to burgeon in the present state of the electronic systems art. It is therefore fitting to explore the fundamental circuit concepts and theories that underlie the design of broadbanded amplifiers and narrowband amplifiers tuned to high radio frequencies. To this end, the feedback network and signal flow theories that clarified the analysis and design of operational amplifiers in the preceding chapter can be gainfully exploited herewith to formulate practical high frequency design strategies. Although MOS technology is of primary interest in the following sections of material, the concepts disclosed apply equally well to virtually all monolithic device technologies, inclusive of bipolar, silicon-germanium (SiGe) heterostructure bipolar, and III-V compound transistors.

The topological foundations of a number of classic broadband analog circuit architectures are studied in this chapter. All of these configurations exploit one or both of two fundamental observations addressed, albeit peripherally, in previous chapters. The first of these observations is that negative feedback applied around a dominant pole open loop produces a closed loop exuding improved frequency response. Indeed, the closed loop

3-dB bandwidth of such a feedback arrangement is larger than the 3-dB bandwidth of the open loop by a factor of one plus the zero frequency value of the loop gain. Unfortunately, single pole open loop amplifiers are indigenous only to the rarified academic climate of a classroom. As the damping factor associated with the interaction of the dominant pole and the unavoidable higher frequency poles of an active network diminishes, the bandwidth improvement afforded by feedback becomes progressively less pronounced. Moreover, the bandwidth enhancement that is realized may be compromised by undesirable frequency response peaking within the passband and even potential circuit instability. Pragmatic limits to the bandwidth benefits incurred by negative feedback are accordingly suggested. In the pages that follow, these limits are studied, and methods to counteract them are developed and exemplified.

The second observation derives from the fact that the 3-dB bandwidth of a dominant pole amplifier having no finite frequency zeros is approximately the inverse sum of the open circuit time constants established by the energy storage elements within the amplifier. Although the open circuit time constant method of estimating bandwidth is a straightforwardly applied and even insightfully useful tool for high frequency circuit assessment, its utility as a broadbanding design vehicle is limited from several perspectives. First, the method suggests that broadbanding a dominant pole network reduces to the problems of determining the designable parameters that determine the frequency of the dominant pole and then adjusting an appropriate subset of these variables to incur an increased pole frequency. To some extent, this engineering strategy is viable. But the frequencies of the presumably nondominant network poles are invariably influenced by any parametric perturbations. Even if these other frequencies are magically unaffected, progressive successes recorded with respect to increasing the dominant pole frequency result ultimately in a nondominant pole circuit for which a bandwidth estimate predicated on pole dominance is erroneous. In short, moving the dominant pole to higher frequencies means that the originally dominant pole is displaced to a region of the complex frequency plane that is populated by higher order poles.

A second limitation, which is particularly evident in a network whose only energy storage elements are capacitors, is that a displacement of a dominant pole to a higher frequency entails reducing the effective open circuit resistance “seen” by one or more of the network capacitors. Such a design tack invariably entails either a reduction of shunt I/O port resistances or/and an increase in device transconductances, both of which mandate increases

in circuit biasing currents. The increased circuit power dissipation typified by these types of broadbanding strategies forebodes battery longevity problems in portable electronic systems.

The third issue is more the result of an analytical restriction than it is an actual limitation. In particular, the open circuit time constant method of predicting bandwidth is premised on the nonexistence of finite frequency zeros, in addition to the presence of a dominant pole. Consider compensating an amplifier whose dominant pole has a radial frequency of p by introducing a zero at radial frequency z . If z is within a factor of the square root of two of p , the high frequency amplifier response never attenuates to 3-dB below its zero frequency gain. Accordingly, the compensated amplifier boasts infinitely large 3-dB bandwidth, despite the fact that the strict application of the open circuit time constant method predicts a finite 3-dB bandwidth of p . The inference of the foregoing elementary disclosure is that the uncompensated bandwidth of p might be appreciably extended, not by increasing p but rather, by introducing a finite zero into the amplifier transfer function to mitigate the effects of the dominant pole. In the sections that follow, broadband compensation via the introduction of zeros receives considerable attention.

9.2.0. Cascade of Dominant Pole Amplifiers

The majority of broadbanding schemes address the individual gain stages of an electronic network. A design-oriented concentration on individual stages is logical in the sense that the response of an overall electronic network can be no faster than is its slowest constituent. The fact that the gain requirements in most high frequency applications are rarely satisfied by a single amplification stage bodes the necessity of a cascade of presumably broadbanded individual network stages. Questions therefore arise as to the effects exerted by cascading on the resultant observable 3-dB bandwidth of the system.

To the foregoing end, assume an electronic network comprised of a cascade of N stages, each of which boasts an n th order transfer function of

$$H(s) = \frac{H(0)}{\left(1 + \frac{s}{p_1}\right) \left(1 + \frac{s}{p_2}\right) \left(1 + \frac{s}{p_3}\right) \cdots \left(1 + \frac{s}{p_n}\right)}, \quad (9-1)$$

where $H(0)$ represents the zero frequency, or “DC,” gain of the stage, p_1 through p_n are the radial frequencies of the network poles, and no finite

frequency zeros are evidenced. It is worthwhile interjecting that the method of open circuit time constants delivers a radial bandwidth estimate, B , deriving from

$$\frac{1}{B} \approx \sum_{i=1}^n \frac{1}{p_i}, \quad (9-2)$$

which represents little more than the s -term coefficient in the algebraic expansion of the denominator on the right hand side of Eq. (9-1). It is also worth noting for future reference that while Eq. (9-2) is only an approximation of the actual 3-dB bandwidth, the right hand side of Eq. (9-2) is precisely the zero frequency value of the amplifier envelope delay. This metric is the time delay of the output response, measured with respect to the input excitation, in the sinusoidal steady state.

Let the stage in question be designed to ensure that the pole at $s = -p_1$ is dominant. This assumption implies that p_1 is a real number and that the product, $|H(0)|p_1$, closely approximates the unity gain frequency of the stage. It also implies that $|H(0)|p_1$ is smaller than the magnitude of any of the remaining pole frequencies, p_2 through p_n . The upshot of these stipulations is that (9-1) collapses to

$$H(s) \approx \frac{H(0)}{\left(1 + \frac{s}{p_1}\right)}, \quad (9-3)$$

and, by Eq. (9-2), the 3-dB bandwidth becomes $B \approx p_1$. Note that the aforementioned product, $|H(0)|p_1$, is the gain-bandwidth product, GBP , of the stage at hand and that this product converges toward the unity gain radial frequency, ω_u , of the stage; that is,

$$GBP \triangleq |H(0)|B \approx |H(0)|p_1 \approx \omega_u. \quad (9-4)$$

9.2.1. Bandwidth of N -Stage Cascade

A cascade of N stages, each characterized by the transfer relationship in Eq. (9-3) produces an overall transfer function, $H_T(s)$, given by

$$H_T(s) = H^N(s) = \frac{H^N(0)}{\left(1 + \frac{s}{p_1}\right)^N}, \quad (9-5)$$

assuming that the input port of any one stage does not appreciably load the output port of its predecessor stage. One way of precluding interstage

loading effects entails a design wherein the magnitude of the driving point input impedance of each stage is much larger than that of the stage output port within the signal passband of interest. A more practical way of mitigating loading effects at high signal frequencies is to design each stage for matched and constant driving point input and output resistances. More information is tendered later on broadbanding via constant resistances.

In the sinusoidal steady state, Eq. (9-5) becomes

$$H_T(j\omega) = H^N(j\omega) = \frac{H^N(0)}{\left(1 + \frac{j\omega}{B}\right)^N}, \quad (9-6)$$

where use is made of the fact that the 3-dB frequency of a dominant pole circuit is the frequency of said pole. The cascaded 3-dB bandwidth resultantly derives from the requirement,

$$\left[1 + \left(\frac{B_T}{B}\right)^2\right]^{N/2} = \sqrt{2}, \quad (9-7)$$

whence

$$\frac{B_T}{B} = \sqrt{2^{1/N} - 1}, \quad (9-8)$$

which suggests bandwidth compression in a cascade configuration. For example, a cascade of two identical stages produces a bandwidth that is 35.6% smaller than the 3-dB bandwidth of any single stage.

A more utilitarian form of Eq. (9-8) derives from the observation that

$$2^{1/N} = e^{\ln(2^{1/N})} = e^{\ln 2/N}. \quad (9-9)$$

But for large N ,

$$2^{1/N} = e^{\ln 2/N} \approx 1 + \frac{\ln 2}{N}, \quad (9-10)$$

which, when combined with Eq. (9-8), delivers

$$\frac{B_T}{B} = \sqrt{2^{1/N} - 1} \approx \sqrt{\frac{\ln 2}{N}}. \quad (9-11)$$

For $N \geq 2$, Eq. (9-11) predicts a normalized bandwidth that is low by no more than 8.53%, which is close enough for government work. A slight computational error notwithstanding, the advantage of Eq. (9-11) is that it suggests that the overall bandwidth of a cascade diminishes as roughly the square root of the number of cascaded stages. This observation is interesting

in that Eq. (9-6) confirms that the decibel value of cascaded zero frequency gain rises linearly with the number of stages. Accordingly, the decibel gain value rises with N faster than the overall system bandwidth degrades, which suggests that acceptably high amplifier bandwidths can be achieved through prudent design measures, despite system requirements that drive a need for additional stages.

9.2.2. Optimized Bandwidth of a Cascade

The dependence of gain and bandwidth on the number of cascaded identical stages warrants further exploration. To this end, assume an N stage cascade whose overall gain magnitude at zero signal frequency is a given value, say K . It follows that each identical stage of the amplifier must deliver a gain magnitude at zero frequency of $K^{1/N}$, which implies an individual stage gain-bandwidth product of $GBP = K^{1/N} B$. Using Eq. (9-11), the overall bandwidth, B_T , of the cascade configuration is expressible as

$$B_T \approx B \sqrt{\frac{\ln 2}{N}} = \frac{GBP}{K^{1/N}} \sqrt{\frac{\ln 2}{N}}. \quad (9-12)$$

Figure 9.1 plots the normalized overall bandwidth, B_T/GBP , as a function of the number of stages, N , for various values of the overall gain, K . For a fixed gain-bandwidth product, GBP , in each of the identical stages and a given overall gain magnitude specification, K , this 3-dB bandwidth expression is clearly a nonmonotonic function of N . It displays a maximum value, say B_{T_o} , at a particular value of N , which can be denoted as N_o . Note that the actual maximum overall bandwidth is somewhat soft in the sense that B_T is not an especially sensitive function of N for relatively large values of N and K . The number, N_o , can be determined by equating the derivative of B_T with respect to N in Eq. (9-12) to zero. The result of this unpleasant task is

$$N_o = \ln(K^2), \quad (9-13)$$

which defines the optimum number of stages commensurate with a given cascade gain specification. The corresponding zero frequency gain of each stage in the cascade is relatively small and is, in particular,

$$H(0) = K^{1/N_o} = \sqrt{e}, \quad (9-14)$$

where e is the base of natural logarithms. Upon insertion of Eq. (9-13) into

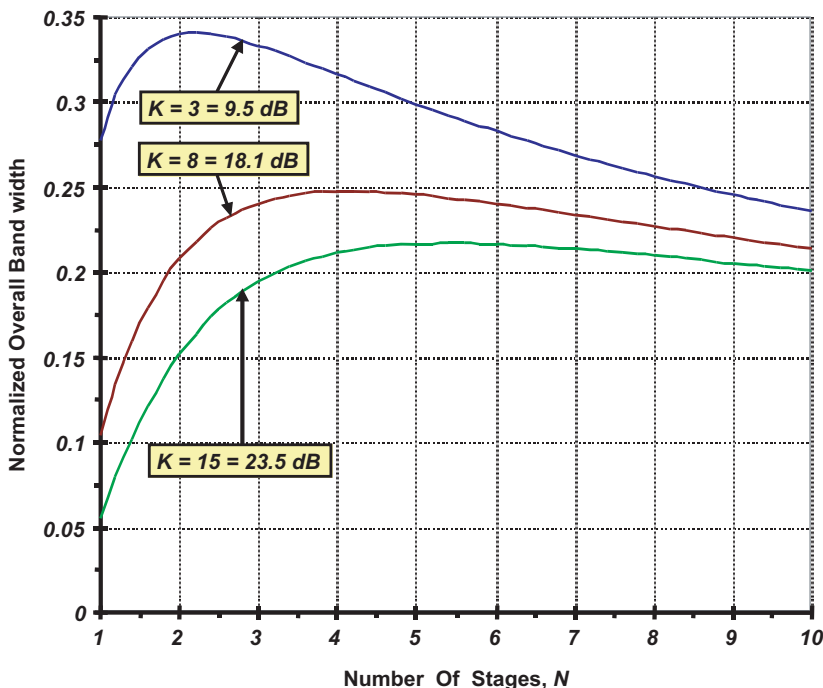


Figure 9.1. The overall bandwidth of a cascade of N identical stages as a function of the number of stages, N , for three values of the overall DC gain, K . The overall bandwidth on the vertical scale of this plot is normalized to the gain-bandwidth product of a single amplification stage.

Eq. (9-12), the maximum possible 3-dB bandwidth is found to be

$$B_T = GBP \sqrt{\frac{\ln 2}{2e \ln K}}. \quad (9-15)$$

Example 9.1. A low frequency gain magnitude of at least 6 is required of a lowpass amplifier that is to be designed to deliver a 3-dB frequency of 1.5 GHz. If this amplifier is to be realized as a cascade of a number of identical stages, determine the optimum number of stages and the corresponding 3-dB bandwidth to which each stage must be designed if maximum overall bandwidth is to be achieved.

Solution 9.1.

(1) From Eq. (9-13), an overall gain of 6 commands that the number of stages be $N_o = 3.584$. Since the realization of a cascade comprised of a non-integral

- number of stages is a daunting challenge, choose $N_o = 4$, which implies a revised gain magnitude design goal of $K = e^{4/2} = 7.389 = 17.4$ dB.
- (2) With $B_T = 1.5$ GHz and $K = 7.389$, Eq. (9-15) stipulates a gain-bandwidth product for each stage of $GBP = 5.941$ GHz.
 - (3) Since the optimized gain-per-stage is the square root of the base of natural logarithms, or 1.649, the requisite 3-dB bandwidth of each dominant pole stage is $B = GBP/1.649 = 3.60$ GHz.

Comments. The simplicity of these computations warrants no further explanation, but the numerical results are enlightening in that they paint a somewhat foreboding design scenario. While a single example hardly posits generalized and reliable design guidelines, it appears that bandwidth optimization in cascaded, identical dominant pole stages has dubious broadbanding merit. In particular, observe that the bandwidth requirement of each stage in this example is 140% of the system bandwidth goal of 1.5 GHz. This stage bandwidth is doubtlessly attainable with state of the art monolithic processes, particularly since the gain magnitude of each stage is only 1.649, or 4.34 dB. However, four stages are required to produce a gain magnitude of only 7.389. The extant state of the art boasts monolithic transistors having unity gain frequencies in the mid-tens of gigahertz. It may therefore be more prudent, at least from a power dissipation perspective, to attempt a realization of the performance specifications with either one amplification stage or perhaps two, non-identical stages.

An additional concern is that the transfer function of the final circuit realization effectively projects a fourth order pole at nominally 3.60 GHz. In view of the parasitic feedback invariably confronted in the course of physically implementing the amplifier cascade, this multi-order pole contributes to poor phase and gain margins and possibly, outright instability.

9.3.0. Degenerative RC Broadbanding

In Chapter 6, the frequency response of the common source amplifier is definitively investigated, primarily because the common source stage is the workhorse of MOS technology systems requiring significant I/O gain. Fig. 9.2(a) offers a slight variation to the common source topology in that a degeneration resistance, R_f , is inserted into the source lead of the transistor. As might be expected and as is to be confirmed, this resistance acts as a negative feedback element to extend the 3-dB bandwidth of the basic common source stage at the expense of reducing the stage zero frequency gain. It also allows for the introduction of capacitive compensation that extends the degenerated bandwidth without additional gain penalty. Assuming transistor operation in its saturation regime, Fig. 9.2(b) is the pertinent small signal

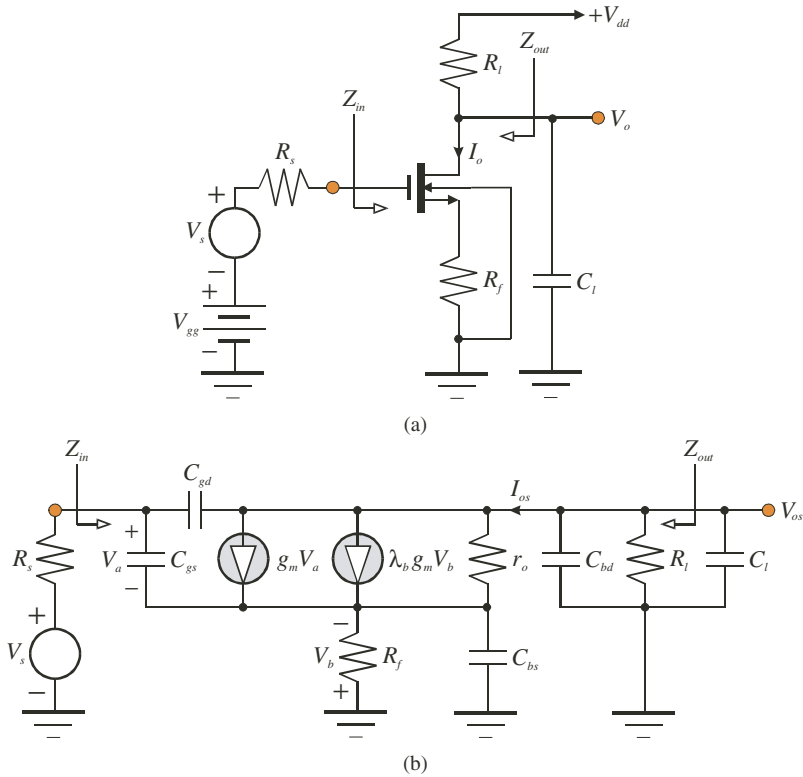


Figure 9.2. (a) Basic schematic diagram of a common source amplifier in which a source degeneration resistance, R_f , is used to establish negative feedback. (b) Small signal, high frequency model of the amplifier in (a). The transistor is presumed biased in saturation.

model, where resistance R_l is the drain load resistance, C_l is the net capacitance loading the amplifier output port, and R_s is the Thévenin resistance of the signal source. The transistor is represented by its traditional small signal parameters. In particular, g_m is the forward transconductance, λ_b is the bulk transconductance factor, r_o is the small signal channel resistance, C_{gs} is the gate-source capacitance, C_{gd} is the gate-drain capacitance, C_{bd} is the bulk-drain capacitance, and finally, C_{bs} symbolizes the bulk source capacitance.

9.3.1. Gain and Dominant Pole

Figure 9.3(a) diagrams the small signal low frequency version of the model in Fig. 9.2(b). In this low frequency equivalent circuit, the feedback

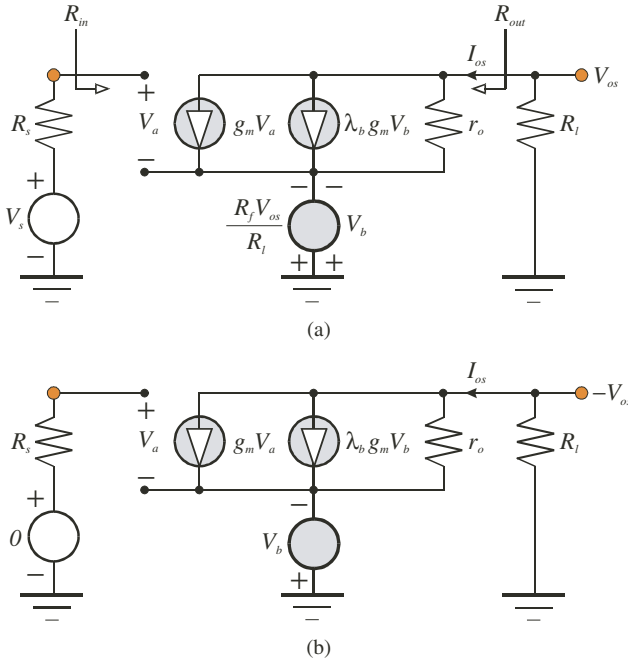


Figure 9.3. (a) The low frequency version of the small signal equivalent circuit offered in Fig. 9.2(b). (b) The model of (a) configures for the computation of the normalized return ratio with respect to the feedback factor, R_f/R_l .

resistance, R_f , is supplanted by a voltage controlled voltage source, $-R_f V_{os}/R_l$, where use is made of the fact that the small signal load current, $I_{os} = -V_{os}/R_l$, flows through the resistance, R_f , which is embedded in the source lead of the transistor. This replacement of a resistance by a controlled voltage source makes clear that the feedback factor at low signal frequencies is R_f/R_l , and that the low frequency, open loop (in the sense of $R_f = 0$) voltage gain, $A_o(0)$, is

$$A_o(0) = \left. \frac{V_{os}}{V_s} \right|_{R_f=0} = -g_m (r_o \parallel R_l) \approx -g_m R_l, \tag{9-16}$$

where the approximation reflects the tacit, but generally reasonable, assumption that $r_o \gg R_l$.

Figure 9.3(b) reconfigures the model in Fig. 9.3(a) for the express purpose of evaluating the low frequency normalized return ratio, $Q_s(0)$, with respect to the feedback factor. A straightforward circuit analysis confirms that

$$Q_s(0) = \left. \frac{V_{os}}{V_b} \right|_{V_s=0} = (1 + \lambda_b)g_m(r_o \parallel R_l) + \frac{R_l}{R_l + r_o}. \quad (9-17)$$

Since the feedback generator is controlled by the output voltage response variable, the null return ratio with respect to the feedback parameter is itself null. Accordingly, the low frequency loop gain, $T(0)$, evolves as

$$T_s(0) = \left(\frac{R_f}{R_l} \right) Q_s(0) = \left(\frac{R_f}{R_l + r_o} \right) [1 + (1 + \lambda_b)g_m r_o]. \quad (9-18)$$

If, in addition to $r_o \gg R_l$, $g_m r_o \gg 1$ and $\lambda_b \ll 1$, this expression simplifies to

$$T_s(0) = \left(\frac{R_f}{R_l} \right) Q_s(0) \approx g_m R_f. \quad (9-19)$$

It follows that the low frequency closed loop voltage gain of the amplifier at hand is

$$A(0) = \frac{V_{os}}{V_s} = \frac{A_o(0)}{1 + T_s(0)} \approx -\frac{g_m R_l}{1 + g_m R_f} \approx -\frac{R_l}{R_f}, \quad (9-20)$$

which, assuming $g_m R_f \gg 1$, is essentially independent of transistor parameters. The approximations leading to Eqs. (9-19) and (9-20) require a suitably large MOSFET transconductance, which may command a relatively large gate aspect ratio and/or an appreciable drain bias current. However, care must be exercised to preclude a large drain current from jeopardizing the presumption that the channel resistance, r_o , is substantially larger than the drain load resistance, R_l .

Note that the immediate impact of the degeneration resistance is an attenuation of the common source low frequency gain by a factor of nominally, $(1 + g_m R_f)$. Gain attenuation is to be expected since the applied signal source in the circuit of Fig. 9.2(a) is not impressed across the gate-source terminals of the transistor, as it is in a traditional common source stage. Instead, the signal is applied from the gate terminal to ground, an electrical path that includes the series embodiment of the feedback degeneration resistance, R_f . If the input signal is small enough to cause an insignificant perturbation of the gate-source quiescent voltage, most of the signal, V_s , is developed across resistance R_f . This action results in a signal current, V_s/R_f , flowing in the transistor source lead and since the gate current is

zero at low frequencies, the same signal current flows into the transistor drain terminal and through the drain load resistance, R_f . Consequently, an output signal voltage of $-R_f V_s / R_f$ is developed at the amplifier output port, whence the approximate gain given by Eq. (9-20). It might therefore be asserted that the validity of the approximation in Eq. (9-20) is premised on negligible signal swing induced by signal V_s in the gate-source biasing voltage. This signal swing is tantamount to the error signal observed in a generalized feedback system model. Recall from preceding chapters that this error signal is indeed small in negative feedback systems when the loop gain is sufficiently large.

A first order investigation of the frequency response of the degenerated common source amplifier derives from an examination of the open circuit time constants associated with each capacitance in the model of Fig. 9.2(a). The cumbersome topology of this model renders this task algebraically daunting unless the circuit implications of the approximations noted above are exploited a priori. In particular, a negligibly small transconductance factor, λ_b , means that the controlled source, $\lambda_b g_m V_b$, can be vanquished. On the other hand, a large channel resistance, r_o , renders feasible the removal of the shunt loading imposed by resistance r_o . To these ends, it can be shown that the open circuit time constant, τ_{gs} , associated with the transistor gate-source capacitance, C_{gs} , is (with the implicit understanding that all other capacitances in the model are open circuited)

$$\tau_{gs} = \frac{(R_s + R_f) C_{gs}}{1 + T_s(0)} \approx \frac{(R_s + R_f) C_{gs}}{1 + g_m R_f}, \quad (9-21)$$

where use is made of the approximation projected by Eq. (9-19). It should be noted that in the absence of a source circuit degeneration resistance, R_f , this gate-source time constant is simply $R_s C_{gs}$. An inspection of Eq. (9-21) suggests that a potentially significant reduction in the value of this nondegenerated time constant is manifested by the utilized feedback. In particular and despite the fact that resistance R_f superimposes with the Thévenin source resistance, R_s , in the numerator of the subject expression, the gate-source time constant is diminished by virtue of the fact that the actual gate-source capacitance is effectively reduced by a factor of one plus the zero frequency value of the amplifier loop gain.

An analysis similar to that executed for the gate-source capacitive time constant yields expressions for the open circuit time constants associated

with the remaining capacitances in the model. For the gate-drain capacitance, C_{gd} , the time constant, τ_{gd} , is

$$\tau_{gd} = \left[R_l + \left(1 + \frac{g_m R_l}{1 + g_m R_f} \right) R_s \right] C_{gd}. \tag{9-22}$$

The incorporated feedback resistance is seen to limit the Miller multiplication of the gate-drain capacitance, but it has no effect on the time constant component attributed to the interaction of the load resistance with this capacitance. Thus, feedback is seen to reduce the time constant associated with the gate-drain capacitance to varying degrees, depending on the value of the Thévenin source resistance.

For the bulk-source capacitance, C_{bs} , the open circuit time constant, τ_{bs} , is

$$\tau_{bs} = \frac{R_f C_{bs}}{1 + T_s(0)} \approx \frac{R_f C_{bs}}{1 + g_m R_f}, \tag{9-23}$$

which is again rendered small because of the effective reduction of capacitance C_{bs} by a factor of one plus the zero frequency loop gain. Finally, the net load capacitance, which is the sum of the transistor bulk-drain capacitance, C_{bd} , and the actual load capacitance, C_l , generates an open circuit time constant, τ_l , of

$$\tau_l = R_l (C_{bd} + C_l). \tag{9-24}$$

Feedback has no effect on the latter time constant, at least within the constraints imposed by the invoked analytical approximations. The reason underlying this discovery derives from the tacit presumption of a very large transistor channel resistance, r_o . In particular, large r_o means that the load resistance is driven by a controlled current source whose inherently high terminal resistance effectively isolates the feedback resistance in the source circuit from the load termination.

Assuming that a dominant pole prevails in the amplifier of Fig. 9.2(a), the 3-dB bandwidth, say B_d , of the degenerated amplifier can be approximated as the inverse sum of the four time constants evaluated above. Ignoring those time constant components that are inherently small by virtue of their respective inverse dependence on the zero frequency loop gain,

$$B_d \approx \frac{1}{\tau_{gs} + \tau_{gd} + \tau_{bs} + \tau_l} \approx \frac{1}{R_l (C_{gd} + C_{bd} + C_l) + R_s C_{gd}}. \tag{9-25}$$

In an active RC network, a necessary condition for pole dominance is that one, and only one, capacitive time constant be dominant in comparison to all other computed open circuit time constants. It is hardly a leap of

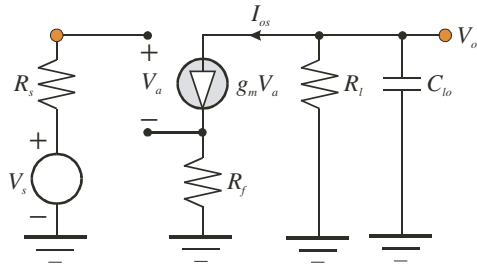


Figure 9.4. Simplified high frequency equivalent circuit of the amplifier in Fig. 9.2(a).

faith to argue that the time constant associated with the output port in the amplifier of Fig. 9.2(a) is the likely root of pole dominance. This contention is particularly germane if the load capacitance, C_l , is purposefully appended to set a particular 3-dB bandwidth that is within the frequency capability of the utilized transistor. Thus, $R_l(C_{gd} + C_{bd} + C_l) \gg R_s C_{gd}$ in Eq. (9-25) is the requirement that forges a dominant pole frequency response. The stipulated inequality is distinctly possible for two reasons. First, the signal source resistance, R_s , is rarely larger than $50\ \Omega$ to $75\ \Omega$ in broadband amplifiers. Second, self-aligning transistor gate technology and transistor saturation combine to render C_{gd} inherently small. It follows that Eq. (9-25) collapses to the simple form,

$$B_d \approx \frac{1}{R_l C_{lo}}, \quad (9-26)$$

where C_{lo} represents the effective load port capacitance “seen” by resistance R_l ; namely,

$$C_{lo} = C_{gd} + C_{bd} + C_l. \quad (9-27)$$

Equations (9-26) and (9-20) combine to establish the simplified high frequency model depicted in Fig. 9.4, for which the closed loop voltage gain as a function of complex frequency s is

$$A(s) = \frac{V_{os}}{V_s} = \frac{A_o(s)}{1 + T_s(s)} \approx - \frac{g_m R_l}{(1 + g_m R_f) \left(1 + \frac{s}{B_d}\right)}. \quad (9-28)$$

9.3.2. Broadband Compensation

As expected, Eq. (9-28) confirms that the net load capacitance in the amplifier modeled by Fig. 9.4 incurs a progressively reduced voltage gain with

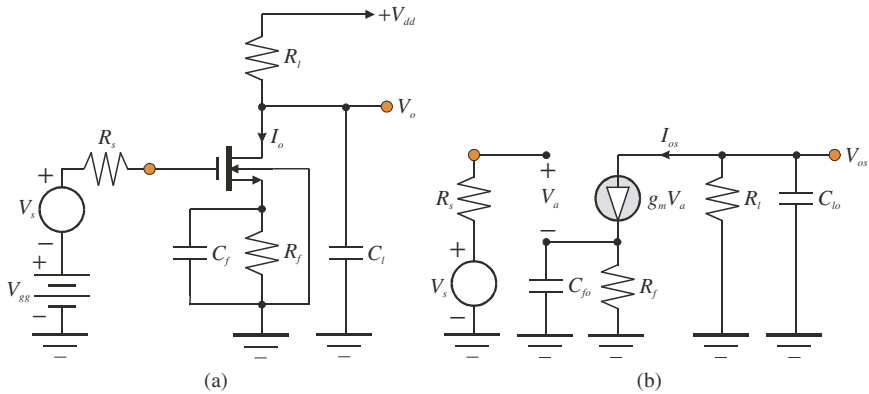


Figure 9.5. (a) Schematic diagram of compensated degenerative amplifier. (b) Small signal, high frequency approximate equivalent circuit of the amplifier in (a).

increasing signal frequency. A possible broadbanding clue derives from the observation that the load capacitance reduces the net load impedance from its zero frequency value of R_L to a value that approaches zero at very high frequencies. Since the gain is nominally proportional to the ratio of the load impedance to resistance R_f , it is logical to consider replacing R_f in the amplifier by a shunt interconnection of R_f and an appropriate capacitance, say C_f , as shown in the schematic diagram of the proposed compensated amplifier in Fig. 9.5(a). To the extent that the gain is directly dependent on the ratio of load impedance to feedback impedance, at least at low signal frequencies, a feedback impedance time constant matched to the time constant of the load impedance allows the feedback impedance to track the load impedance over frequency, whence a broadbanded amplifier frequency response.

The simplified small signal model for the structure in Fig. 9.5(a) appears in Fig. 9.5(b). Since the introduced capacitance, C_f , appears in shunt with the transistor bulk-source capacitance, C_{bs} , capacitance C_{fo} appears in the model, where it is understood that

$$C_{fo} = C_f + C_{bs}. \tag{9-29}$$

If resistance R_f in Eq. (9-28) is now replaced by the parallel combination of R_f and C_{fo} , the transfer function of the compensated amplifier becomes

$$A_c(s) = \frac{V_{os}}{V_s} = \frac{A(0) \left(1 + s R_f C_{fo}\right)}{\left(1 + \frac{s R_f C_{fo}}{1 + g_m R_f}\right) \left(1 + \frac{s}{B_d}\right)}, \tag{9-30}$$

where $A(0)$ is given by Eq. (9-20) and bandwidth B_d of the uncompensated amplifier is defined by Eq. (9-26). If the time constant, $R_f C_{fo}$, established by the net compensation capacitance, C_{fo} , is selected so that it equates to the inverse frequency, $1/B_d$, of the uncompensated dominant pole, the resultant compensated bandwidth, B_c , is

$$B_c = \frac{1 + g_m R_f}{R_f C_{fo}} = (1 + g_m R_f) B_d \approx [1 + T_s(0)] B_d, \quad (9-31)$$

where Eq. (9-19) is exploited. The result indicates that the simple action of appending a capacitance across the feedback resistance in the source lead of the transistor can extend the uncompensated bandwidth by as much as one plus the zero frequency value of the loop gain.

Unfortunately, engineering care must be exercised when interpreting the foregoing result because the pole-zero cancellation on which it is premised is imperfect. In particular, Eq. (9-30) derives from Eq. (9-26), which presumes that pole dominance prevails in the original uncompensated amplifier. Imperfections also abound with respect to equating time constant $R_f C_{fo}$ to inverse B_d . For example, capacitance C_{fo} is a function of transistor bulk-source capacitance C_{bs} , which is rarely known accurately. Moreover, bandwidth B_d relies on capacitance C_{lo} , which in turn is functionally dependent on transistor bulk-drain capacitance C_{bd} , whose precise numerical value, like that of C_{bs} , is elusive. Accordingly, it is at least analytically prudent to investigate the alternative design constraint,

$$R_f C_{fo} = \frac{k}{B_d}, \quad (9-32)$$

with the understanding that the positive number, k , reflects an uncertainty implicit to the desired time constant match. For example, $k = 0.75$ suggests that $R_f C_{fo}$ is 25% smaller than the desired value of $1/B_d$, while $k = 1.25$ implies a 25% larger than desired time constant value. Armed with Eq. (9-32), Eq. (9-30) can be written in the form,

$$\frac{A(s)}{A(0)} = \frac{1 + \frac{sk}{B_d}}{\left\{ 1 + \frac{sk}{[1 + T_s(0)] B_d} \right\} \left(1 + \frac{s}{B_d} \right)}. \quad (9-33)$$

The magnitude response implicit to Eq. (9-33) is plotted in Fig. 9.6 for four values of the constant, k , and a zero frequency loop gain, $T_s(0)$, equal to 10, or 20 dB. The curve for $k = 0$ corresponds to the uncompensated amplifier case and as expected, it projects unity normalized bandwidth (the

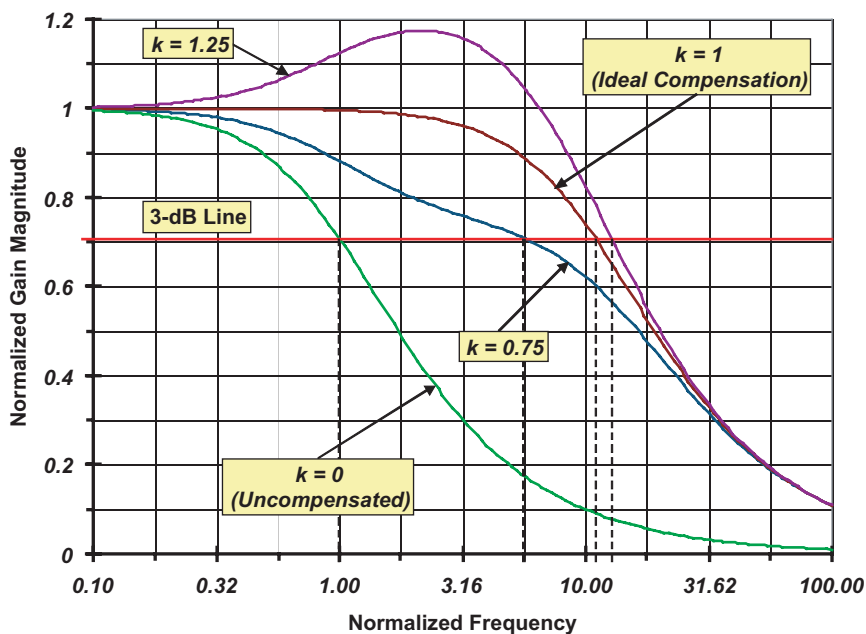


Figure 9.6. Frequency response of the compensated amplifier in Fig. 9.5(a) for a zero frequency loop gain of 10, and various values of k , as defined by Eq. (9.32). The signal frequency is normalized to the bandwidth, B_d , of the uncompensated, degenerated amplifier, while the gain is normalized to the zero frequency value, $A(0)$, of small signal voltage gain.

frequency scale in the plot is normalized to B_d). The $k = 1$ case reflects idealized pole-zero cancellation and shows a normalized bandwidth of 11, which is also expected in view of Eq. (9-31) and the fact that $T_s(0) = 10$. For $k = 1.25$, the normalized compensated bandwidth improves to 12.8, but at the expense of an invariably unacceptable gain peaking of almost 20%. The peaking results because the introduced zero lies at a frequency that is smaller than the frequency of the pole intended for cancellation. Finally, $k = 0.75$ results in a compensated bandwidth that is almost 50% smaller than the bandwidth corresponding to $k = 1$. Note also that the pole-zero doublet resulting from imperfectly cancelled critical frequencies is plainly evident in the normalized frequency range of nominally 1 to 5. The upshot of the matter is that the compensated frequency response is sensitive to the degree by which pole-zero cancellation is actually achieved. A pragmatic mitigation of this sensitivity may entail incorporating a capacitance adjustment capability in either capacitance C_l or C_f to fine-tune the ultimately realized frequency response.

Example 9.2. When suitably biased in saturation, the transistor in the amplifier of Fig. 9.5(a) delivers the following small signal parameters.

Forward Transconductance (g_m):	34 mS
Bulk Transconductance Factor (λ_b):	0.09
Drain-Source Channel Resistance (r_o):	15.8 K Ω
Gate-Source Capacitance (C_{gs}):	173 fF
Gate-Drain Capacitance (C_{gd}):	15 fF
Bulk-Drain Capacitance (C_{bd}):	12 fF
Bulk-Source Capacitance (C_{bs}):	10 fF

Prior to incorporating the feedback resistance, R_f , and its shunting capacitance, C_f , in the circuit, which is driven by a 50 Ω (R_s) signal source, the measured 3-dB bandwidth is 175 MHz, while the measured gain-bandwidth product is determined to be 7 GHz. The desired closed loop bandwidth is 1.5 GHz. Design the circuit by determining the appropriate values of resistance R_f , resistance R_l , capacitance C_f , and capacitance C_l . Using the small signal model provided in Fig. 9.2(b), simulate the small signal frequency response of the finalized design on HSPICE. Examine these responses for the case in which the compensation capacitance, C_f , is 20% smaller than the value required for precise cancellation of the zero forged by the feedback subcircuit and the dominant pole of the uncompensated version of the amplifier.

Solution 9.2.

- (1) If the uncompensated amplifier is characterized by a dominant pole response, a gain-bandwidth product of 7 GHz and a 3-dB bandwidth of 175 MHz implies a zero frequency voltage gain of $|A(0)| = GBP/B_d = 40$. Using Eq. (9-16) with $g_m = 34$ mS and $r_o = 15.8$ K Ω , the requisite drain circuit resistance is $R_l = 1,271$ Ω .
- (2) Recalling Eq. (9-25), $B_d = 2\pi(175 \text{ MHz})$, $R_l = 1,271$ Ω , $R_s = 50$ Ω , $C_{gd} = 15$ fF, and $C_{bd} = 12$ fF deliver a terminating load capacitance of $C_l = 687.9$ fF.
- (3) The factor by which the uncompensated bandwidth is to be enhanced is 1.5 GHz/175 MHz, or 8.571. To first order, this means that $g_m R_f$, by Eq. (9-31), is 7.571, whence $R_f = 7.571/3$ mS = 222.7 Ω . It should be noted that a bandwidth improvement by a factor of 8.571 implies gain degradation by nominally the same amount. Accordingly, the magnitude of voltage gain for the compensated circuit is $|A_c(0)| = |A(0)|/8.571 = 4.667$.
- (4) Recalling Eq. (9-32), $R_f = 222.7$ Ω , $B_d = 2\pi(175 \text{ MHz})$, and $k = 1$ for precise pole-zero cancellation give $C_{fo} = 4.084$ pF. It follows from Eq. (9-29) that with $C_{bs} = 10$ fF, $C_f = 4.074$ pF. A 20% smaller capacitance implies $C_f = 3.259$ fF.
- (5) Figure 9.7 shows the small signal model of the finalized design for the case of precise pole-zero cancellation. The simulated magnitude and phase responses for $k = 1$ appear in Fig. 9.8.

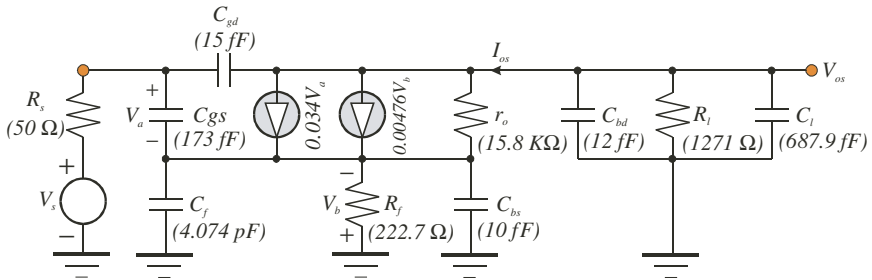


Figure 9.7. Small signal, high frequency equivalent circuit of the amplifier designed in Example 9.2.

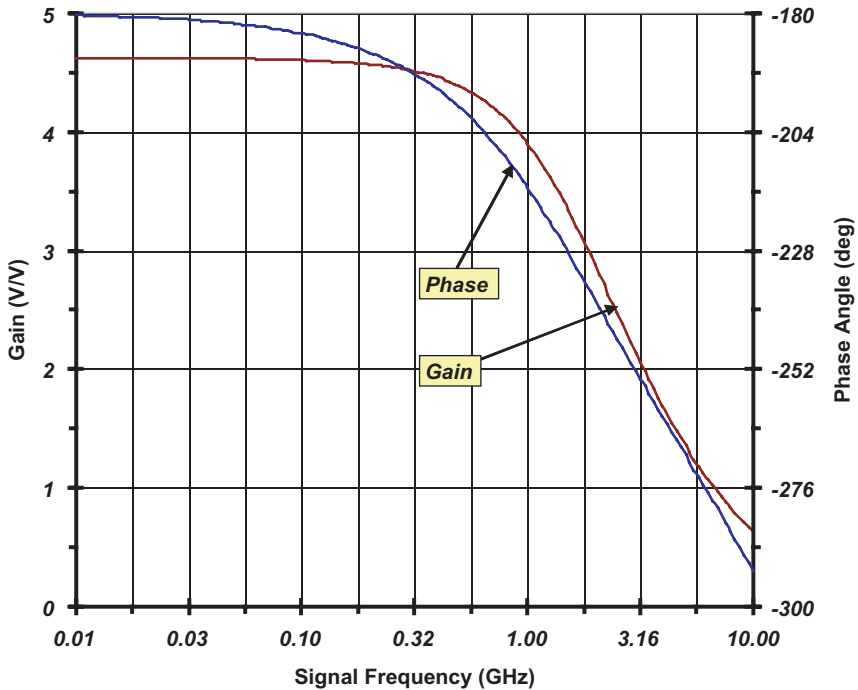


Figure 9.8. The simulated (HSPICE) magnitude and phase responses for the network whose small signal model appears in Fig. 9.7.

Comments. Although the simulated responses given in Fig. 9.8 track well with the foregoing computations, a few minor errors are apparent. These are to be expected in light of the approximations tacitly invoked in the foundational theoretical disclosures. For example, the simulated low frequency voltage gain

is 4.623 volts/volt, which is a scant 0.94% lower than the calculated value of 4.667 volts/volt. Additionally, the simulated bandwidth is 1.589 GHz, which is larger than the 1.5 GHz objective by 5.93%. When C_f is replaced by its 20% smaller value, the 3-dB bandwidth falls to under 1.1 GHz, and a clear pole-zero doublet is evidenced in the magnitude response.

It is worthwhile interjecting that the three-place precision invoked on the model element values has dubious engineering merit in light of the tolerances routinely encountered in manufacturing processes. This precision is invoked herewith merely to demonstrate the engineering propriety of the theoretic background for the computations documented above.

9.4.0. Shunt Peaked Compensation

The preceding section of material dramatizes the positive impact exerted on the frequency response of a common source amplifier by a suitable left half plane zero introduced into the amplifier transfer function. In the foregoing discussion, the requisite zero is forged through shunt RC impedance degeneration inserted into the transistor source terminal. Unfortunately, several costs accompany the laudable bandwidth enhancement afforded by source RC degeneration. The first of these costs is the increased power dissipation resulting from a drain biasing current that necessarily flows through the resistance inserted in the transistor source lead. A second cost is decreased voltage gain. Recall that the closed loop gain is smaller than the amplifier open loop gain (gain with zero resistance in the source terminal) by an amount that roughly equals the bandwidth improvement factor afforded by the incorporated feedback subcircuit. In other words, the gain-bandwidth products of the uncompensated and the compensated amplifiers remain nominally the same, thereby implying that gain is traded for enhanced bandwidth. Finally, resistance in the transistor source lead degrades the noise characteristics of the amplifier. Although a discussion of electronic noise phenomena is beyond the scope of this textbook, suffice it to assert presently that a resistance in the source lead of a common source amplifier increases the equivalent input noise voltage. This noise voltage is a critical amplifier parameter in that it defines the minimum input signal level that can be detected reliably and processed faithfully by the network.

Fortunately, a few alternative means of incorporating transmission zeros into the transfer function of a common source amplifier mitigate most of the foregoing shortfalls. One such method, known as *shunt peaking*, installs the requisite zero through use of an inductor inserted into the transistor drain circuit, as depicted in Fig. 9.9. To be sure, shunt peaking does not result in

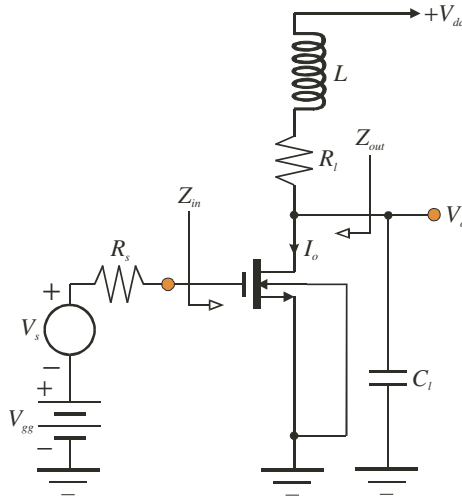


Figure 9.9. Basic schematic diagram of a shunt peaked common source amplifier. The transistor operates in its saturation regime.

a bandwidth enhancement that is as dramatic as that boasted by appropriate source degeneration. But the bandwidth improvement is nonetheless substantial and is afforded without compromising the zero frequency gain of the amplifier. It is therefore notable that shunt peaking delivers increased bandwidth by actually increasing the gain-bandwidth product of the uncompensated, common source configuration. A further advantage of shunt peaked compensation is, ignoring the small winding resistance implicit to the realization of the inductor, that the introduced inductance incurs no increase in static circuit power dissipation. Although inductor winding resistance is detrimental to circuit power dissipation, the quality factor of the utilized inductor, which can be poor in silicon monolithic realizations, is inconsequential to the small signal dynamics of the shunt peaked amplifier because the inductance is inserted in series with the drain load resistance.

9.4.1. Common Source Stage Revisited

Shunt peaking, as diagrammed in Fig. 9.9, is an effective broadbanding strategy, provided that the net capacitance incident at the output port, which includes the indicated load capacitance, C_l , and appropriate transistor capacitances, establishes the dominant time constant in the uncompensated (meaning $L = 0$) amplifier. To this end, a tacit re-investigation

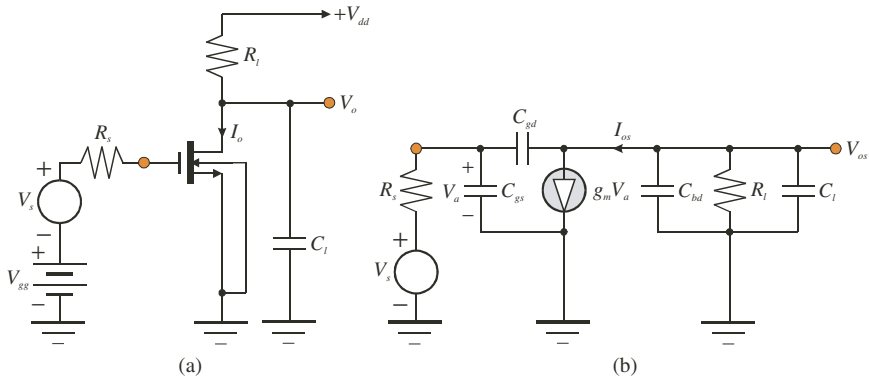


Figure 9.10. (a) Schematic diagram of a simple common source amplifier. The transistor is biased in saturation. (b) Approximate small signal, high frequency model of the network in (a). Drain-source channel resistance and bulk-induced threshold voltage modulation are tacitly ignored.

of the frequency response of the simple common source stage depicted in Fig. 9.10(a) is warranted. The pertinent equivalent circuit shown in Fig. 9.10(b) tacitly neglects the drain-source channel resistance of the transistor.

The zero frequency gain projected by the model in Fig. 9.10(b) is clearly identical to the expression postured by Eq. (9-16); namely, $A(0) = V_{os}/V_s = -g_m R_l$. The time constant analyses executed in the preceding section of material can be gainfully exploited to arrive at the individual open circuit time constants for the model at hand. In particular, with R_f set to zero, Eqs. (9-21), (9-22) and (9-24) give for the respective time constants associated with capacitances C_{gs} , C_{gd} , and C_l ,

$$\tau_{gs} = R_s C_{gs}, \tag{9-34}$$

$$\tau_{gd} = [R_l + (1 + g_m R_l) R_s] C_{gd}, \tag{9-35}$$

and

$$\tau_l = R_l (C_{bd} + C_l). \tag{9-36}$$

If pole dominance prevails, the bandwidth, say B_{cs} , of the common source amplifier derives from

$$\frac{1}{B_{cs}} \approx R_s [C_{gs} + (1 + g_m R_l) C_{gd}] + R_l (C_{gd} + C_{bd} + C_l). \tag{9-37}$$

This result clearly suggests “Miller time” if the gain magnitude, $g_m R_l$, is large and/or the gate-drain capacitance is insufficiently small to warrant its

neglect. Therefore, the load port time constant can be postured as dominating the 3-dB bandwidth estimate if and only if the signal source resistance, R_s , is small, $g_m R_l$ is small, and/or transistor gate self alignment renders capacitance C_{gd} inconsequential. If the load port indeed establishes the dominant time constant, the relevant small signal model reduces to the structure proffered in Fig. 9.11, where capacitance C_{lo} remains given by Eq. (9-27). Accordingly, the 3-dB bandwidth, B_{cs} , of the uncompensated (meaning $L = 0$) common source amplifier is given by the approximate relationship,

$$B_{cs} \approx \frac{1}{R_l C_{lo}}. \tag{9-38}$$

When the dreaded Miller multiplication of the gate-drain capacitance in the common source transistor observably influences the 3-dB bandwidth of the uncompensated circuit, the common source-common gate cascode configuration diagrammed in Fig. 9.12 may prove advantageous, albeit at the expense of an increase in requisite static power dissipation. Since the effective load resistance seen by the common source transistor, $M1$, is nominally the inverse of the transconductance, g_{m2} of the common gate device, $M2$, the Miller multiplier in Eq. (9-37) becomes $(1 + g_{m1}/g_{m2})$ for the stage at hand. If $1/g_{m2} \ll R_l$, which requires that transistor $M2$ be realized with a suitably large gate aspect ratio, the first term on the right hand

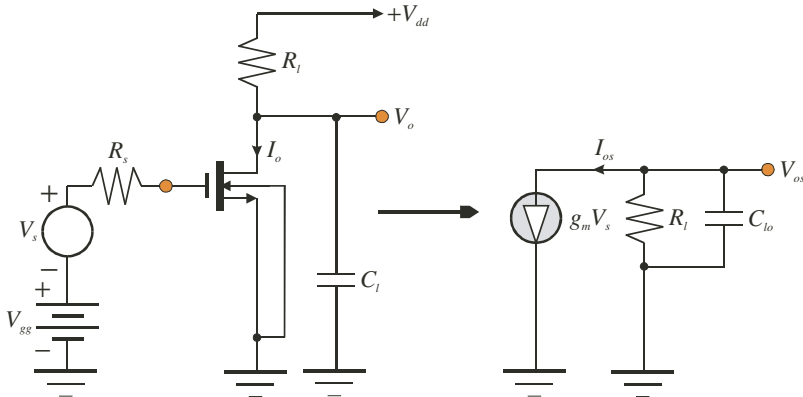


Figure 9.11. Simplified high frequency model of the common source amplifier. The simplification relies on presumed pole dominance established at the output port of the amplifier. The capacitance, C_{lo} , is given by $(C_l + C_{bd} + C_{gd})$.

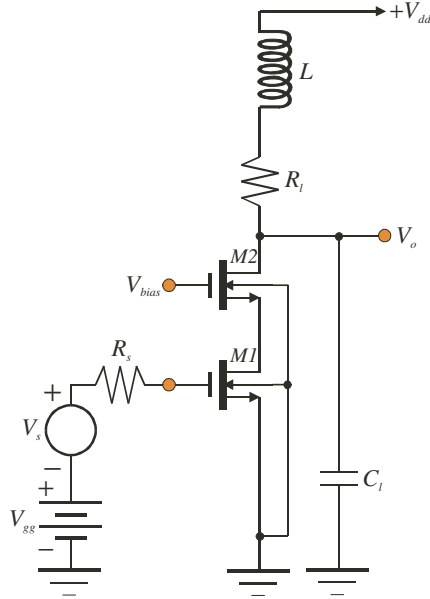


Figure 9.12. A shunt peaked amplifier utilizing a common base cascode, $M2$, to mitigate the effects of Miller multiplication of the gate-drain capacitance in the common source transistor, $M1$.

side of Eq. (9-37) is significantly diminished, thereby allowing the amplifier dominant pole to be established at the load port of the amplifier. To be sure, the inclusion of transistor $M2$ manifests additional time constants that are not embodied by Eq. (9-37). For example, the bulk-drain capacitance of $M1$, as well as the bulk-source and gate-source capacitances of $M2$, faces an effective resistance of roughly $1/g_{m2}$, which, as noted above, is presumably small. It should be observed that the capacitances, C_{gd} and C_{bd} , embedded in the second term on the right hand side of Eq. (9-37) now correspond respectively to the gate-drain and bulk-drain capacitances of transistor $M2$. Because the form factor of $M2$ is invariably larger than that of transistor $M1$, thereby giving rise to increased device capacitances, the second term on the right hand side of Eq. (9-37) is likely to be slightly larger than the value evidenced in the simple common source amplifier of Fig. 9.9. Nonetheless, the common gate current buffer likely improves the overall bandwidth because of the potentially dramatic reduction of Miller multiplication of the gate-drain capacitance in the common source driver.

9.4.2. Shunt Peaked Amplifier Response

In the shunt peaked stage in Fig. 9.9 or the cascode version shown in Fig. 9.12, the amplifier driving the load comprised of capacitance C_l in shunt with the series interconnection of resistance R_l and inductance L emulates a transconductor. If the resistively terminated transconductor functions as a dominant pole amplifier whose dominant pole frequency is determined by the net capacitance, C_{lo} , incident at the load port, the pertinent small signal equivalent circuit is the structure suggested in Fig. 9.13. An inspection of

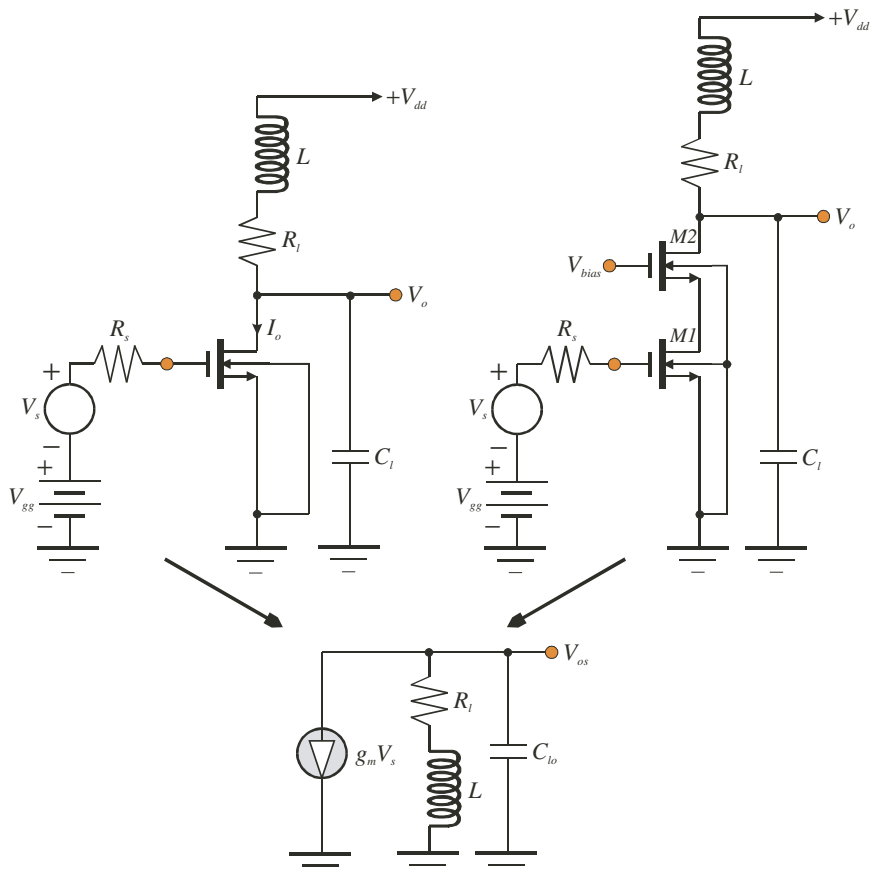


Figure 9.13. Approximate small signal, high frequency model of a common source or a common gate cascode shunt peaked amplifier. The indicated model presumes pole dominance established at the output port when inductance L is zero.

the subject diagram reveals a voltage gain, $A(s)$, of

$$A(s) = \frac{V_{os}}{V_s} = -\frac{g_m R_l \left(1 + \frac{sL}{R_l}\right)}{1 + sR_l C_{lo} + s^2 L C_{lo}}. \quad (9-39)$$

Not surprisingly, the zero frequency voltage gain is $A(0) = -g_m R_l$. If gain $A(s)$ is normalized to this zero frequency value, Eq. (9-39) can be cast in the form,

$$A_n(s) \triangleq \frac{A(s)}{A(0)} = \frac{1 + \frac{Qs}{\omega_n}}{1 + \frac{s}{Q\omega_n} + \left(\frac{s}{\omega_n}\right)^2}, \quad (9-40)$$

where $A_n(s)$ denotes the normalized voltage gain function,

$$\omega_n = \frac{1}{\sqrt{L C_{lo}}} \quad (9-41)$$

is the undamped natural frequency of the circuit, and, recalling Eq. (9-38),

$$Q = \frac{1}{\omega_n R_l C_{lo}} = \frac{B_{cs}}{\omega_n} = \frac{\sqrt{L/C_{lo}}}{R_l} \quad (9-42)$$

is the circuit quality factor. It should be understood that the undamped natural frequency, ω_n , is the frequency at which inductance L resonates with capacitance C_{lo} under the zero damping circumstance of a null circuit resistance, R_l . Moreover, the quality factor, Q , is the quality factor of the circuit inductance at frequency ω_n ; that is, $Q \equiv \omega_n L / R_l$. Equations (9-40) through (9-42) confirm that the insertion of the inductance in the drain load circuit of the uncompensated topology establishes a left half plane zero that can be exploited for broadbanding purposes. Unfortunately, Eq. (9-40) also suggests that the compensated structure may exhibit undue frequency response peaking. The obvious source of this peaking is the left half plane zero, which can lie at too low a frequency within the circuit passband if Q is too large and/or ω_n is too small. The second, and more subtle, cause of unacceptable peaking is that complex circuit poles, which arise for $Q > 1/2$, conduce underdamped responses.

The foregoing and related other issues are best examined by expressing the normalized gain in Eq. (9-40) as an explicit function of a complex

frequency, say p , that is normalized to the bandwidth, B_{cs} , of the uncompensated amplifier; that is, the amplifier prior to insertion of the peaking coil. Thus, with

$$p \triangleq s / B_{cs}, \tag{9-43}$$

Eq. (9-40) becomes

$$A_n(p) \triangleq \frac{A(p)}{A(0)} = \frac{1 + Q^2 p}{1 + p + Q^2 p^2}. \tag{9-44}$$

In the sinusoidal steady state, the complex frequency, p , can be replaced by jy , with the understanding that y represents radial signal frequency, ω , normalized to bandwidth B_{cs} . With $y \triangleq \omega / B_{cs}$,

$$A_n(jy) \triangleq \frac{A(jy)}{A(0)} = \frac{1 + jQ^2y}{1 - (Qy)^2 + jy}. \tag{9-45}$$

Figure 9.14 displays a plot of the magnitude response implied by Eq. (9-45) for three values of the circuit quality factor. Observe that for $Q = 1$, almost 50% peaking is evidenced, while the amount of peaking diminishes rapidly

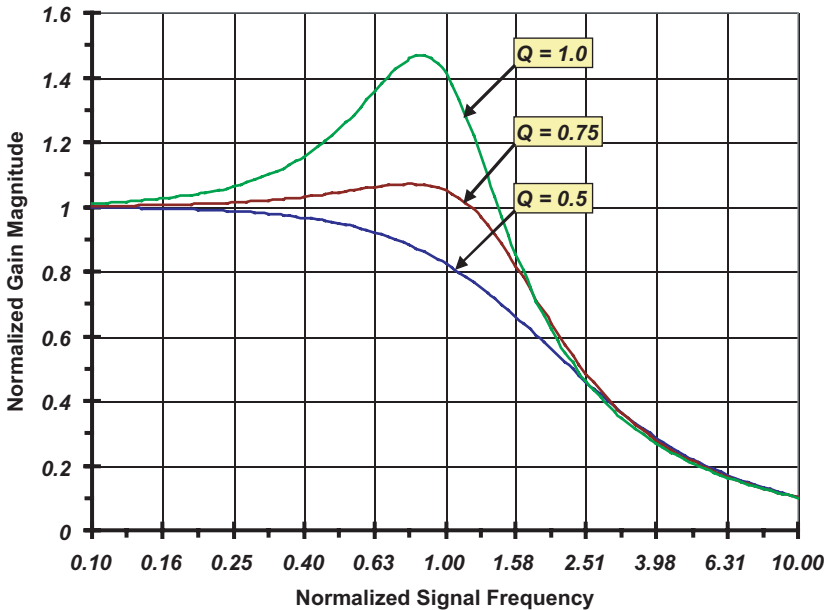


Figure 9.14. Magnitude response, plotted for various values of the circuit quality factor, Q , of the shunt peaked amplifier modeled in Fig. 9.13.

with progressive decreases in Q . Note further that the 3-dB bandwidth, which is the normalized frequency yielding a gain magnitude of the inverse of root two, increases with increasing Q .

9.4.2.1. Maximally Flat Magnitude Response

Figure 9.14 teaches the apparent existence of an optimum quality factor such that maximal bandwidth is attained within the constraint of a flat response exhibiting no peaking within the amplifier passband. This optimality is tantamount to the condition of a maximally flat magnitude (MFM) frequency response, for which the first $(N - 1)$ frequency derivatives of the magnitude response for an N th order system are identically null at zero frequency. For such a system, it can be shown that the normalized squared magnitude response, $|H_N(jy)|^2$, must mirror the general form,^[1]

$$|H_N(jy)|^2 = \frac{P(y^2)}{P(y^2) + a_N y^{2N}}, \quad (9-46)$$

where $P(y^2)$ is an even order polynomial in the squared normalized frequency variable, y^2 , and a_N is a constant. Observe that this general expression suggests a squared magnitude response whose form is the ratio of a polynomial divided by the identical polynomial plus one additional, frequency dependent term. From Eq. (9-45),

$$|A_n(jy)|^2 = \frac{1 + Q^4 y^2}{1 + (1 - 2Q^2) y^2 + Q^4 y^4}, \quad (9-47)$$

which mirrors the MFM form of Eq. (9-46), provided that the quality factor, Q , satisfies

$$Q^4 = 1 - 2Q^2. \quad (9-48)$$

The positive solution of Eq. (9-48), which stipulates the specific quality factor, say Q_m , commensurate with maximal flatness of shunt peaked amplifier response, is

$$Q_m = \sqrt{\sqrt{2} - 1} = 0.6436. \quad (9-49)$$

While Eq. (9-49) stipulates an optimized quality factor in the sense of achieving a MFM response, the bandwidth achieved by this optimal condition is not immediately apparent. There is some room for concern in this regard since maximal flatness attained with a compensated 3-dB bandwidth that is less than its uncompensated value has dubious merit. To this end,

return to Eq. (9-47) to set the squared magnitude transfer function equal to $1/2$ at a normalized frequency, say y_b , where y_b represents the ratio of compensated bandwidth, say B_l , to the uncompensated bandwidth, B_{cs} . The fruit of an hour or two of depressing algebra is

$$y_b = \frac{B_l}{B_{cs}} = \sqrt{\frac{(2Q^4 + 2Q^2 - 1) + \sqrt{(2Q^4 + 2Q^2 - 1)^2 + 4Q^4}}{2Q^4}}. \quad (9-50)$$

For the quality factor given by Eq. (9-49), Eq. (9-50) delivers $y_b = 1.722$, which infers a laudable 72.2% increase in the uncompensated circuit bandwidth when the shunt peaking inductor is selected to ensure a maximally flat magnitude response.

It is essential to underscore the fact that Eq. (9-49) does not deliver maximum possible bandwidth in the compensated structure. Instead, it yields maximum bandwidth within the constraint of no peaking of the observable frequency response. This contention is highlighted by Fig. 9.15, which plots y_b in Eq. (9-50) as a function of the circuit quality factor, Q . This

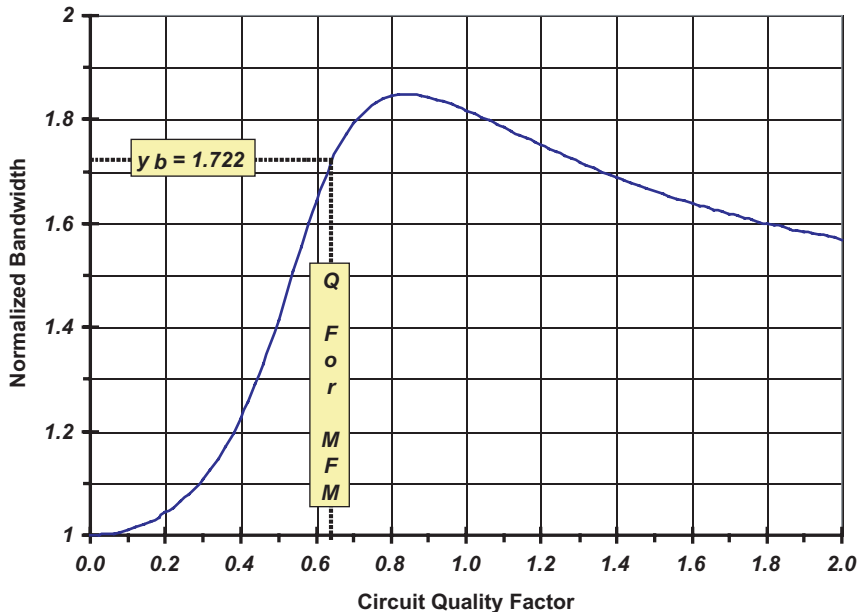


Figure 9.15. The bandwidth, normalized to the uncompensated circuit bandwidth, of the shunt peaked amplifier. A quality factor of $Q = 0.6436$ ensures a maximally flat magnitude response delivering a 72.2% improvement in circuit bandwidth.

figure infers an attainable bandwidth improvement approaching 85% in the neighborhood of $Q = 0.86$. Unfortunately, the price paid for this additional bandwidth enhancement is a peaked response, since, as Fig. 9.14 verifies, peaking becomes progressively more pronounced as the circuit quality factor increases.

In order to assess quantitatively the extent of the aforementioned peaking, the derivative, with respect to normalized frequency y , of the squared magnitude function in Eq. (9-47) can be equated to zero to ascertain the value of y , say y_m , where maximal squared gain is evidenced. The requisite mathematics are hardly enjoyable, but a closed form solution for y_m can be determined; namely, the nonzero value of y_m is

$$y_m = \frac{\sqrt{Q\sqrt{Q^2+2}-1}}{Q^2}. \quad (9-51)$$

Since y_m is a particular frequency normalized to the 3-dB bandwidth of the uncompensated circuit, it must obviously be a real number. The relationship at hand projects real y_m if and only if

$$Q\sqrt{Q^2+2} \geq 1, \quad (9-52)$$

which requires $Q \geq 0.6436 \equiv Q_m$. Thus, frequency response peaking is evidenced only for circuit quality factors that exceed the quality factor commensurate with the realization of a maximally flat magnitude response. For $Q = Q_m$, y_m in Eq. (9-51) is zero, which is as expected, since a maximally flat magnitude frequency response implies the existence of a response maximum at only zero frequency.

Yet another immensely enjoyable exercise entails substituting Eq. (9-51) into Eq. (9-47) to discern the maximum value, say M , of the normalized magnitude response. The result, which is meaningful only when $Q \geq Q_m$, is

$$M|_{Q \geq Q_m} = |A_n(jy_m)|_{Q \geq Q_m} = \frac{Q^2}{\sqrt{2Q\sqrt{Q^2+2} - (2Q^2+1)}}. \quad (9-53)$$

For $Q < Q_m$, M is understood to be one. This understanding reflects the fact that for small Q , no peaking in excess of the zero frequency gain magnitude arises at nonzero frequencies, thereby implying that maximum gain, whose normalized value is one, is observed at only zero frequency. The percentage overshoot, obtained simply by multiplying $(M - 1)$ by 100, is plotted in Fig. 9.16. It is a bit distressing to note that this overshoot is a somewhat sensitive function of quality factor. To wit, zero percent overshoot is ensured for $Q = Q_m = 0.6436$, but at $Q = 0.775$, almost 10%

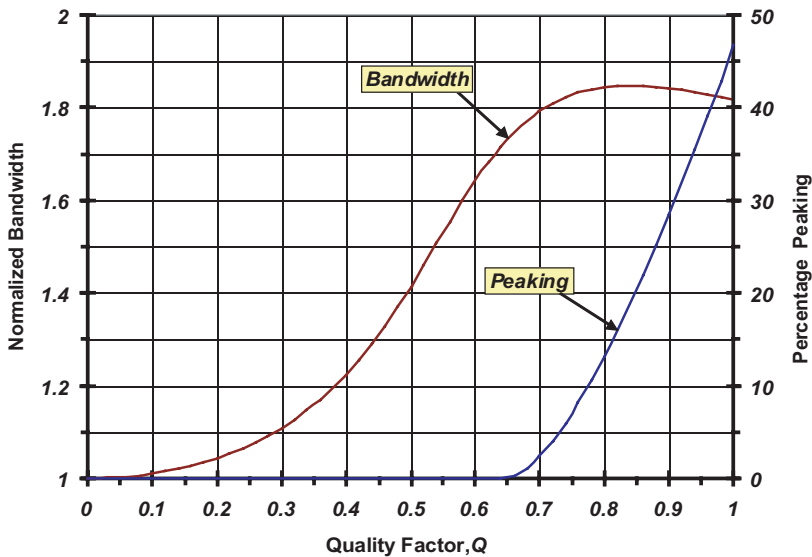


Figure 9.16. The bandwidth, normalized to the uncompensated circuit bandwidth, and the percentage peaking in the frequency response of the shunt peaked amplifier in Fig. 9.13.

overshoot prevails. In contrast, the normalized bandwidth increases only slightly over this Q -interval, from 1.722 at $Q = 0.6436$ to 1.838 at $Q = 0.775$.

Example 9.3. The inductor in the amplifier of Fig. 9.9 is to be selected to ensure a maximally flat magnitude frequency response. This response is to be characterized by a zero frequency gain of 18 dB and a 3-dB bandwidth of at least 1.6 GHz when the amplifier is driven by a 50Ω signal source. The utilized transistor is the same as the device exploited in Example 9.2; its small signal model parameters are repeated herewith for reader convenience.

Forward Transconductance (g_m):	34 mS
Bulk Transconductance Factor (λ_b):	0.09
Drain-Source Channel Resistance (r_o):	15.8 K Ω
Gate-Source Capacitance (C_{gs}):	173 fF
Gate-Drain Capacitance (C_{gd}):	15 fF
Bulk-Drain Capacitance (C_{bd}):	12 fF
Bulk-Source Capacitance (C_{bs}):	10 fF

Design the circuit by determining the appropriate values of the peaking inductance, L , the drain load resistance, R_l , and the requisite load capacitance, C_l . Using the small signal model provided in Fig. 9.2(b), simulate the small signal frequency

response of the finalized design on HSPICE. Compare the frequency response of the compensated amplifier with that of the uncompensated ($L = 0$) version.

Solution 9.3.

- (1) The bandwidth enhancement afforded by a maximally flat, shunt peaked amplifier response is 72.2%. Thus, if the compensated bandwidth is to be at least 1.6 GHz, the bandwidth of the stage without inductive compensation must be no smaller than $1.6 \text{ GHz}/1.722 = 929.1 \text{ MHz}$. To allow for the various approximations invoked in the course of shunt peaked response analysis, it is prudent to design the uncompensated stage for a 3-dB bandwidth of 950 MHz; that is, $B_{cs} = 2\pi(950 \text{ MHz})$.
- (2) A voltage gain of 18 dB is equivalent to a numerical gain of 7.943. Since the zero frequency magnitude of voltage gain is $g_m(r_o \parallel R_l)$, the required drain load resistance is $R_l = 237.1 \Omega$.
- (3) Equation (9-38) is an applicable expression for the 3-dB bandwidth of the uncompensated amplifier. A slightly more accurate relationship is

$$B_{cs} = \frac{1}{(r_o \parallel R_l) C_{lo}}, \quad (\text{E3-1})$$

whence, $C_{lo} = 717.1 \text{ fF}$. Recalling Eq. (9-27) and the gate-drain and bulk-drain capacitances given above, the load capacitance terminating the output port of the amplifier follows as $C_l = 690.1 \text{ fF}$.

- (4) Using Eq. (9-42), the required inductance value of the shunt peaking coil is

$$L = (QR_l)^2 C_{lo}. \quad (\text{E3-2})$$

Recalling that $Q = 0.6436$ for MFM response, $L = 16.70 \text{ nH}$.

- (5) Figure 9.17 delineates the resultant small signal models for both the uncompensated and the shunt peaked compensated amplifiers. The simulated magnitude responses of both of these structures are depicted in Fig. 9.18.

Comments. The HSPICE results pictured in Fig. 9.18 confirm that the zero frequency gain magnitude of both the uncompensated common source amplifier and the shunt peaked common source unit is precisely the design target of nominally 7.94 volts/volt. The simulated frequency response of the uncompensated network shows a 3-dB bandwidth of 913.3 MHz, which is 3.86% lower than the design target of 950 MHz. Correspondingly, the simulated 3-dB bandwidth of the compensated structure is 1.55 GHz, which is 3.13% smaller than the 1.6 GHz design objective. These small errors can be attributed to the numerous approximations invoked to arrive at tractable, design-oriented results.

The quoted differences between simulation results and manual computations are actually smaller than the errors typically experienced in the course of broadband

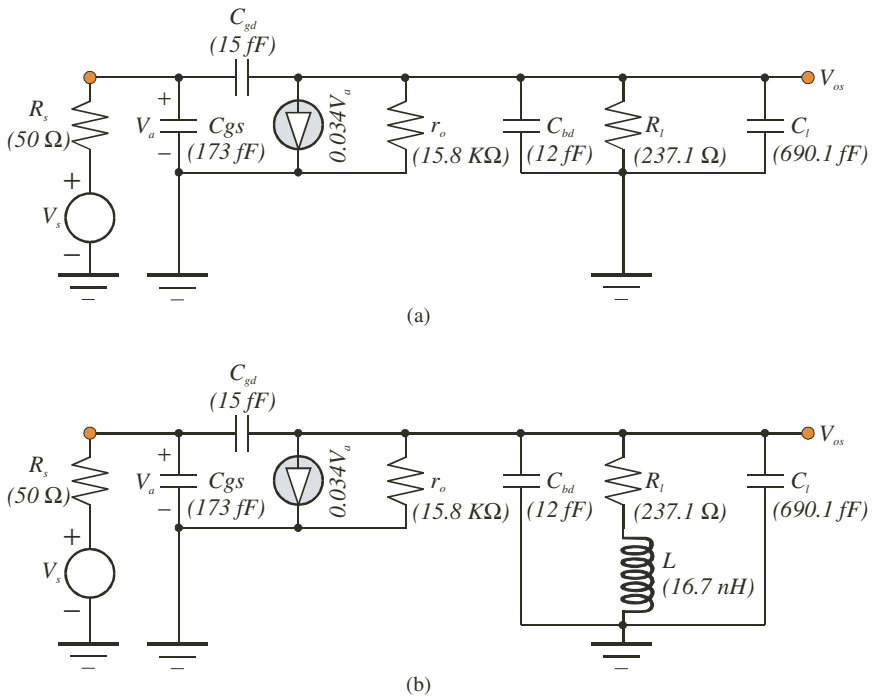


Figure 9.17. (a) Small signal model of the uncompensated amplifier considered in Example 9.3. (b) Small signal model of the shunt peaked common source amplifier designed for maximally flat magnitude response in Example 9.3.

amplifier design in MOSFET technologies. Designable circuit elements can be adjusted to correct for the observed errors. For example, the load capacitance can be decreased to incur a reduction in net capacitance C_{lo} by 3.13%, provided that inductance L is likewise reduced by the same factor to preserve the quality factor required for MFM response. However, these adjustments may comprise an exercise in engineering futility, given routinely encountered manufacturing tolerances with respect to electronic circuit components. In other words, response errors accruing from manufacturing tolerances are likely to be comparable to, or even larger than, those observed herewith.

A final point worthy of mention is that the requisite inductance of 16.7 nH may be too large for practical monolithic implementation. Inductances of at most 4 nH to 6 nH are generally an implicit requirement of monolithic circuit layout. In the present case, the specifications may need to be altered and/or different topological structures may need to be adopted if the ultimately designed circuit is to be realized pragmatically as an analog integrated circuit.

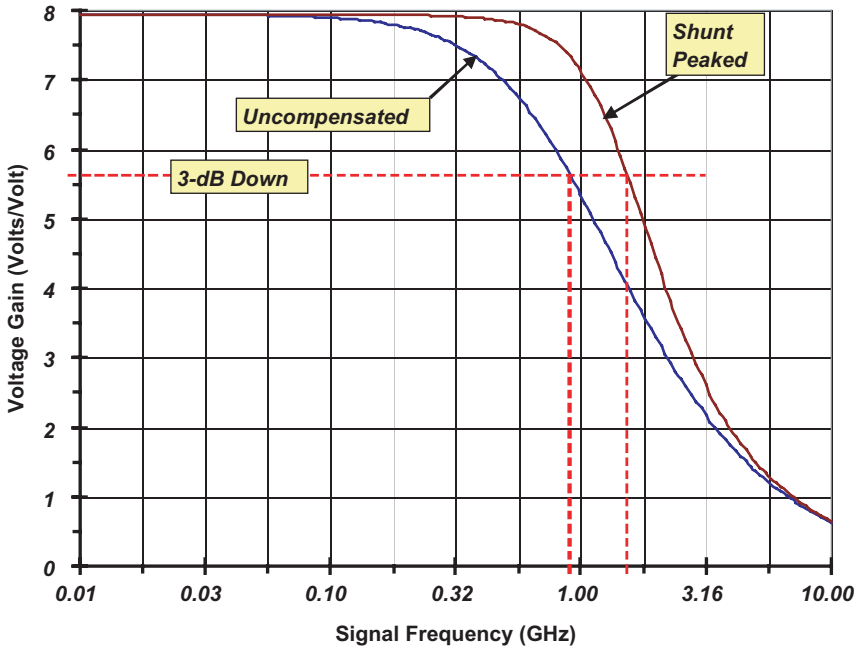


Figure 9.18. The simulated (HSPICE) magnitude responses for the two small signal amplifier models offered in Fig. 9.17.

9.4.2.2. Maximally Flat Delay Response

The realization of a maximally flat, or at least reasonably flat, magnitude response is arguably the most common objective of a circuit broadbanding strategy. But numerous electronic system applications require, in addition to a sufficiently broad passband, the ability to process input signals with nominally constant time delay, independent of the frequency spectrum of these signals. Examples of such applications include high speed electronic instrumentation, video systems, and digital communication systems.^[2] Accordingly, it is prudent to investigate the shunt peaked amplifier from the perspective of its amenability to provide nominally constant I/O signal delay over suitably wide frequency passbands.

Of particular engineering interest is the network time delay achieved in the steady state. This steady state delay is commonly referenced as the *envelope delay*, $D(\omega)$, which relates to the I/O phase response, $\phi(\omega)$ as

$$D(\omega) = -\frac{d\phi(\omega)}{d\omega}. \quad (9-54)$$

If the network transfer function, and thus its phase response, is cast explicitly as a function of a normalized frequency variable, y , as it is in Eq. (9-45) with $y = \omega/B_{cs}$,

$$-\frac{d\varphi(\omega)}{d\omega} = -\frac{1}{B_{cs}} \frac{d\varphi(y)|_{y=\omega/B_{cs}}}{dy} = \frac{D(y)}{B_{cs}}, \tag{9-55}$$

so that

$$D(y) \triangleq -\frac{d\varphi(y)}{dy} = B_{cs} D(\omega)|_{\omega=B_{cs}y} \tag{9-56}$$

is identified as the envelope delay, normalized to a delay value of $1/B_{cs}$.

Returning to Eq. (9-45), the phase response of the compensated shunt peaked network is

$$\varphi(y) = \tan^{-1}(Q^2y) - \tan^{-1}\left[\frac{y}{1 - (Qy)^2}\right]. \tag{9-57}$$

Using Eq. (9-56), the normalized delay function is found to be

$$D(y) = \frac{1 + (Qy)^2}{1 + (1 - 2Q^2)y^2 + Q^4y^4} - \frac{Q^2}{1 + Q^4y^2}. \tag{9-58}$$

Observe a zero frequency normalized delay of $D(0) = (1 - Q^2)$, which is predictable via an inspection of Eq. (9-45). The delay response defined by Eq. (9-58) and plotted in Fig. 9.19 for various values of the circuit quality factor reveals an apparent optimal value of Q , say Q_d , such that the delay is rendered nominally constant over a suitably broad frequency passband.

The MFM concepts addressed previously can be applied to the delay function in the hope of achieving a maximally flat delay (MFD) response. To this end, the criterion underlying MFD response realization derives from an attempt to couch the right hand side of Eq. (9-58) into the form of the right hand side of Eq. (9-46). If Eq. (9-58) is expressed as a ratio of polynomials in the squared normalized frequency variable, y^2 ,

$$D(y) = (1 - Q^2) \times \left[\frac{1 + \left(\frac{3Q^4}{1 - Q^2}\right)y^2}{1 + (Q^4 - 2Q^2 + 1)y^2 + 2Q^4(1 - Q^2)y^4 + Q^8y^6} \right]. \tag{9-59}$$

Because the numerator on the right hand side in this expression is a first order polynomial in y^2 , while the denominator is a third order polynomial

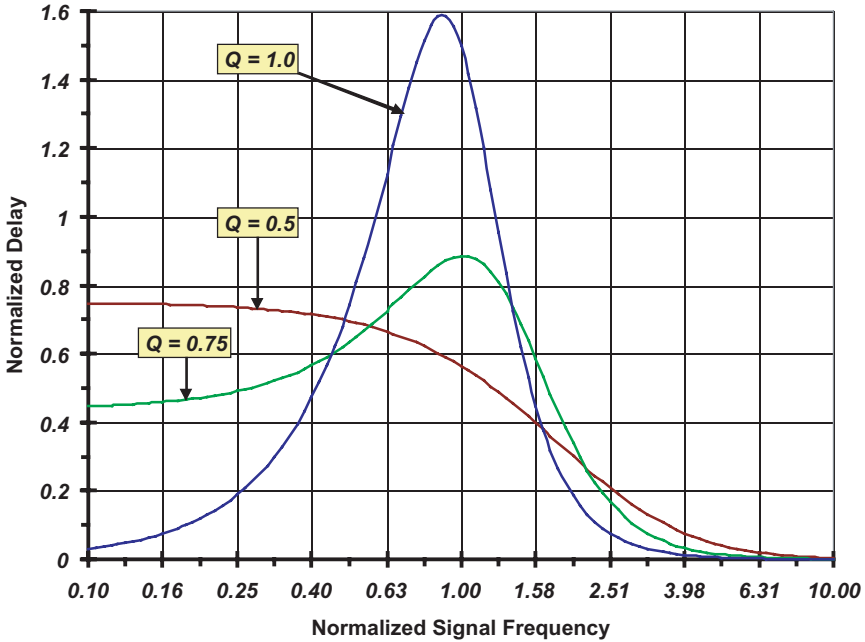


Figure 9.19. The normalized delay response of the shunt peaked amplifier shown in Fig. 9.13.

in y^2 , $D(y)$ cannot be rendered a strictly maximally flat function of y in the sense of the form projected by the right hand side of Eq. (9-46). But MFD can nonetheless be approximated by equating the y^2 coefficients in the numerator and the denominator. Specifically, if Q_d signifies the optimal quality factor commensurate with an approximate MFD response,

$$\frac{3Q_d^4}{1 - Q_d^2} = Q_d^4 - 2Q_d^2 + 1, \tag{9-60}$$

which gives rise to the constraint,

$$Q_d^6 + 3Q_d^2 - 1 = 0. \tag{9-61}$$

Believe it or not, this equation can be solved precisely for Q_d by first changing variables to transform the sixth order relationship to an equivalent cubic.^[3] The positive real root of Eq. (9-61) is

$$Q_d = \sqrt{\sqrt[3]{\left(\frac{\sqrt{5} + 1}{2}\right)} - \sqrt[3]{\left(\frac{\sqrt{5} - 1}{2}\right)}} = 0.5676. \tag{9-62}$$

At least three interesting observations with respect to this result can be proffered. First, no peaking in the magnitude response results from designing for $Q = Q_d$, since peaking is manifested only for $Q > Q_m = 0.6436$. Second, a consideration of the calculations leading to the bandwidth plot in Fig. 9.16 confirms a bandwidth improvement with respect to the uncompensated amplifier of almost 57%. Although this improvement is smaller than the bandwidth enhancement observed under the MFM condition, it is nonetheless laudable in view of the fact that this enhancement derives from the addition of only one, nominally lossless, component to the basic amplifier configuration. Finally, for $y = 1.57$ and $Q = Q_d = 0.5676$, the last term in the denominator on the right hand side of Eq. (9-59) evaluates numerically as 0.1614, which is 6.2-times smaller than unity, the zero frequency value of this denominator polynomial. Of course, the other terms in the subject denominator are themselves positive and hence add to the unity term, thereby making the final term comparatively smaller still. The reasonable engineering conclusion herewith is that MFD over a wide signal passband is well approximated by $Q = Q_d$ in the shunt peaked amplifier.

9.5.0. Series Peaked Compensation

In a shunt peaked amplifier, as diagrammed in Fig. 9.9, the inductive branch is placed in parallel with the amplifier output port to which the net capacitance serving to establish the dominant pole of the uncompensated amplifier is presumed to be incident. In contrast, a series peaked amplifier places the inductive branch in series with the load capacitance, C_l , that the amplifier is compelled to drive. As can be seen in the pertinent schematic diagram of Fig. 9.20(a), the compensating inductance, L , separates the load capacitance from the amplifier output port capacitance, C_o , which is fundamentally the sum of the bulk-drain and gate-drain capacitances associated with the common gate cascode transistor, $M2$. As is demonstrated shortly, the additional capacitance, C_x , appended to the amplifier output port proves indispensable with respect to achieving a broadbanded, maximally flat magnitude response in the compensated structure. The pertinent small signal model, given in Fig. 9.20(b), is premised on two presumptions. First, the drain-source channel resistance of both transistors is sufficiently large to warrant its tacit neglect. Second, with $L = 0$, pole dominance attributed to the net output port capacitance is presumed. Accordingly, the uncompensated

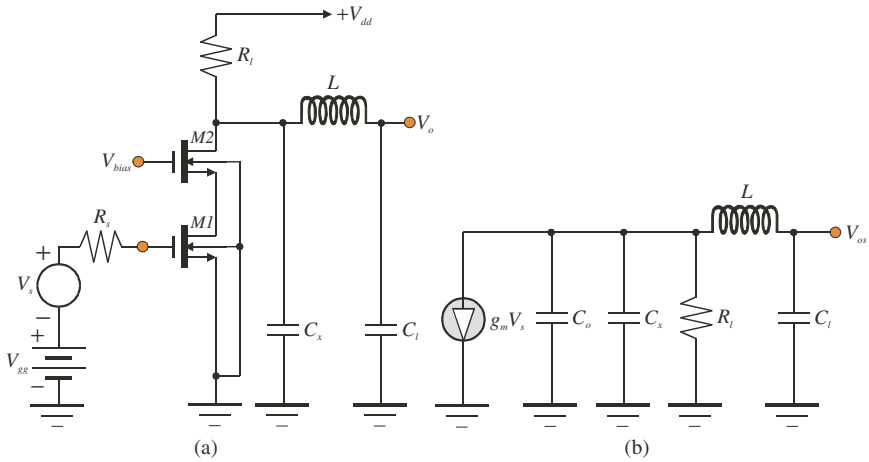


Figure 9.20. (a) Basic schematic diagram of series peaked amplifier. (b) Approximate small signal, high frequency model of the circuit in (a). Both transistors *M1* and *M2* are presumed to operate in saturation, and pole dominance attributed to the net output port capacitance is presumed when $L = 0$.

radial 3-dB bandwidth, B_u , is

$$B_u \approx \frac{1}{R_l (C_o + C_l)}. \tag{9-63}$$

Note that capacitance C_x is not included in this expression, for C_x is a requirement of only the compensated, series peaked topology.

A straightforward analysis of the model in Fig. 9.20(b) sets forth a voltage transfer function of

$$\begin{aligned} A_v(s) &= \frac{V_{os}}{V_s} \\ &= - \frac{g_m R_l}{1 + s R_l (C_o + C_x + C_l) + s^2 L C_l + s^3 L C_l R_l (C_o + C_x)}, \end{aligned} \tag{9-64}$$

where, $-g_m R_l$ is confirmed as the zero frequency value, $A_v(0)$, of the voltage gain. Two special cases are of immediate interest: a compensated second order and a compensated third order response.

9.5.1. Second Order Compensated Response

The series peaking case traditionally visited by much of the textbook literature is the condition in which the capacitance sum, $(C_o + C_x)$ is negligible, whence the normalized gain deriving from Eq. (9-64) reduces to

$$A_n(s) = \frac{A_v(s)}{A_v(0)} = \frac{A_v(s)}{-g_m R_l} = \frac{1}{1 + sR_l C_l + s^2 L C_l}. \quad (9-65)$$

This second order transfer relationship has no finite zeros to enhance its bandwidth attributes. Nonetheless, it produces a maximally flat magnitude response, known as a Butterworth response, when the normalized transfer function abides by the functional form,^[4]

$$A_n(s) = \frac{1}{1 + \frac{\sqrt{2}s}{B_c} + \left(\frac{s}{B_c}\right)^2}, \quad (9-66)$$

where B_c symbolizes the compensated 3-dB bandwidth. By a comparison of this expression with the right hand side of Eq. (9-65), a Butterworth MFM response materializes if

$$\left. \begin{aligned} \frac{\sqrt{2}}{B_c} &= R_l C_l \\ \frac{1}{B_c^2} &= L C_l \end{aligned} \right\}. \quad (9-67)$$

Recalling Eq. (9-63), the time constant, $R_l C_l$, is the inverse of the uncompensated circuit bandwidth, B_u , if C_o is indeed a negligible capacitance. Accordingly, the first of the expressions in Eq. (9-67) suggests immediately that MFM series peaking in the face of negligible capacitance at the amplifier output port improves bandwidth by a factor of the square root of two; that is,

$$B_c = \sqrt{2} B_u. \quad (9-68)$$

Additionally, this result and Eq. (9-67) combine to stipulate a required inductance value of

$$L = \frac{R_l}{2B_u}, \quad (9-69)$$

which highlights a requisite inductance such that its reactance at the uncompensated circuit bandwidth is precisely one-half of the drain load resistance. Equivalently, it can be stated that the quality factor of the shunt peaking

coil at a frequency equaling the uncompensated amplifier bandwidth is precisely $1/2$.

Series peaking endures bad press in comparison to the exaltations showed on shunt peaking largely because of Eq. (9-68), which extols a slightly better than 41% enhancement in uncompensated circuit bandwidth. In contrast, shunt peaking designed for MFM response enhances bandwidth by better than 72%. Since broadbanding by even small amounts is generally a painful design experience, a 41% bandwidth improvement, gleaned without significant static power dissipation penalty, is nonetheless laudable. Series peaking does not deserve the aforementioned negative press. But the approximations underpinning the second order response in Eq. (9-65), which entail the tacit neglect of all capacitances incident at the output port of the uncompensated amplifier, are fair game for vigorous criticism.

9.5.2. Third Order Compensated Response

A third order circuit providing a maximally flat, Butterworth response requires a normalized transfer characteristic of the form,

$$A_n(s) = \frac{1}{1 + 2\left(\frac{s}{B_c}\right) + 2\left(\frac{s}{B_c}\right)^2 + \left(\frac{s}{B_c}\right)^3}, \quad (9-70)$$

where, as in the case in the second order circuit addressed in the preceding subsection, B_c represents the radial 3-dB bandwidth of the compensated amplifier. A term-by-term comparison of this expression with the right hand side of Eq. (9-64) leads to

$$\left. \begin{aligned} \frac{2}{B_c} &= R_l(C_o + C_x + C_l) \\ \frac{2}{B_c^2} &= LC_l \\ \frac{1}{B_c^3} &= LC_l R_l(C_o + C_x) \end{aligned} \right\}. \quad (9-71)$$

When combined with Eq. (9-63), the first of these expressions produces

$$\frac{B_c}{B_u} = \frac{2}{1 + \frac{C_x}{C_o + C_l}}, \quad (9-72)$$

which, assuming $C_x \ll (C_o + C_l)$, portends almost a doubling of the uncompensated circuit bandwidth. From the second expression in Eq. (9-71), the required inductance value is

$$L = \frac{2}{B_c^2 C_l}. \quad (9-73)$$

Finally, the combination of all three expressions in Eq. (9-71) produces the design requirement,

$$C_o + C_x = \frac{C_l}{3}, \quad (9-74)$$

whereupon Eq. (9-72) can be equivalently expressed as

$$\frac{B_c}{B_u} = \frac{3}{2} \left(1 + \frac{C_o}{C_l} \right). \quad (9-75)$$

Obviously, C_o in Eq. (9-75) can be no smaller than zero, while from Eq. (9-74), C_o can be no larger than $C_l/3$. Accordingly, the factor by which the uncompensated circuit bandwidth can be improved via third order, Butterworth MFM compensation is between 1.5 and 2.0. In other words, third order, series peaked bandwidth compensation is guaranteed to be slightly better than that afforded by its second order counterpart and conceivably, it can exceed the bandwidth compensation factor implicit to maximally flat shunt peaked compensation.

Example 9.4. When driven by a 50Ω signal source, a series peaked amplifier is to deliver a maximally flat response characterized by a zero frequency voltage gain of 14 dB and a 3-dB frequency of 2.2 GHz. The utilized transistor is the same as the device exploited in Example 9.3. Design the circuit by determining the appropriate values of the series peaking inductance, L , the drain load resistance, R_l , the requisite load capacitance, C_l , and the compensation capacitance, C_x , required at the amplifier output port. Using the small signal model provided in Fig. 9.2(b), simulate the small signal frequency response of the finalized design on HSPICE. Compare the frequency response of the compensated amplifier with that of its uncompensated version.

Solution 9.4.

- (1) A voltage gain of 14 dB is equivalent to a numerical gain of 5.012. Since the zero frequency magnitude of voltage gain is $g_m(r_o \parallel R_l)$, the required drain load resistance is $R_l = 148.8 \Omega$.

(2) Using Eqs. (9-71) and (9-74),

$$B_c = \frac{3}{2R_l C_l}; \tag{E4-1}$$

With $B_c = 2\pi(2.2\text{GHz})$ and $R_l = 148.8\ \Omega$, the required load capacitance follows as $C_l = 729.3\ \text{fF}$.

- (3) For $C_o = C_{gd} + C_{bd} = 27\ \text{fF}$, Eq. (9-74) yields $C_x = 216.1\ \text{fF}$.
- (4) From Eq. (9-73), the required inductance is $L = 14.35\ \text{nH}$.
- (5) From Eq. (9-75), the bandwidth improvement factor is $B_c/B_u = 1.556$, which means that the bandwidth of the uncompensated amplifier is $B_u = 2\pi(1.41\ \text{GHz})$. It is to be understood that in the present context, “uncompensated” means $L = 0$ and $C_x = 0$.
- (6) Figure 9.21 diagrams the small signal models for both the uncompensated and the series peaked compensated amplifiers. The simulated magnitude responses of both of these structures are provided in Fig. 9.22.

Comments. The HSPICE results portrayed in Fig. 9.22 show a zero frequency gain magnitude for both amplifiers that is nearly precisely equal to the design goal. The simulated 3-dB bandwidth of the compensated amplifier is 2.23 GHz

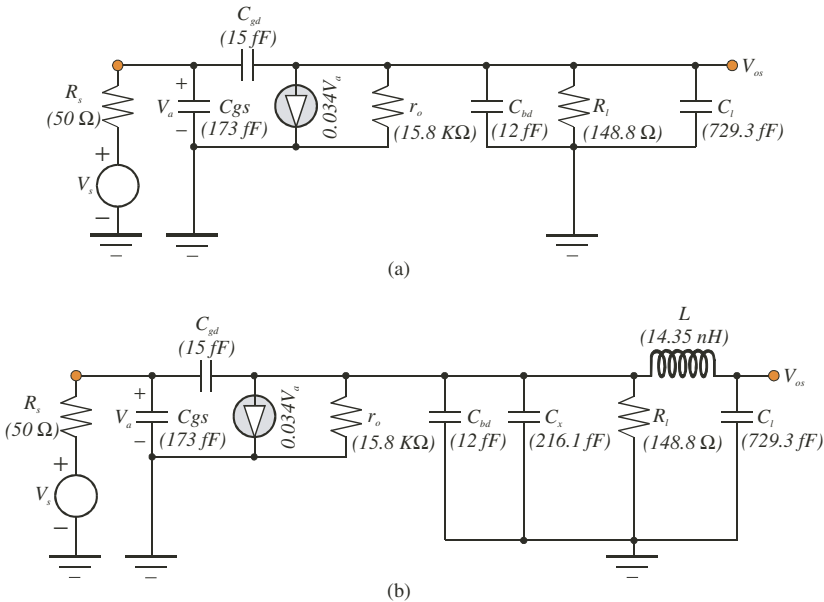


Figure 9.21. (a) Small signal model of the uncompensated common source amplifier addressed in Example 9.4. (b) Small signal model of the series peaked common source amplifier designed for maximally flat magnitude response in Example 9.4.

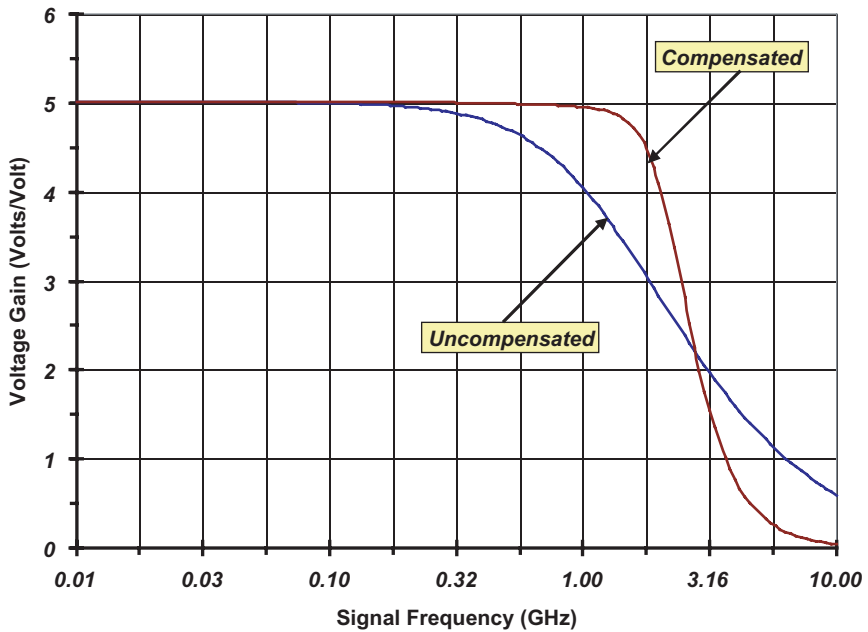


Figure 9.22. The simulated magnitude responses for the small signal models of the uncompensated and the compensated series peaked amplifier shown in Fig. (8.21).

and is once again nearly identical to the design objective. On the other hand, the uncompensated structure shows a 3-dB bandwidth of 1.37 GHz. Thus, the factor by which bandwidth improves as a result of series peaking in this example is $2.23/1.37 = 1.63$, which is higher than the calculated enhancement factor by about 4.5%.

The example at hand conveys no drama with respect to calculated and simulated amplifier performance. It does serve to show that maximally flat magnitude series peaking can be nominally as effective as the more traditionally invoked shunt peaking compensation strategy.

9.6.0. Series-Shunt Peaked Compensation

If shunt peaking and series peaking comprise effecting circuit broadbanding strategies, engineers are naturally inclined to suspect that the marriage of these two techniques may result in even more dramatic frequency response improvements. In order to examine the propriety of this suspicion, consider Fig. 9.23(a), which depicts the schematic diagram of a representative MOS technology series-shunt peaked amplifier driving a load of pure

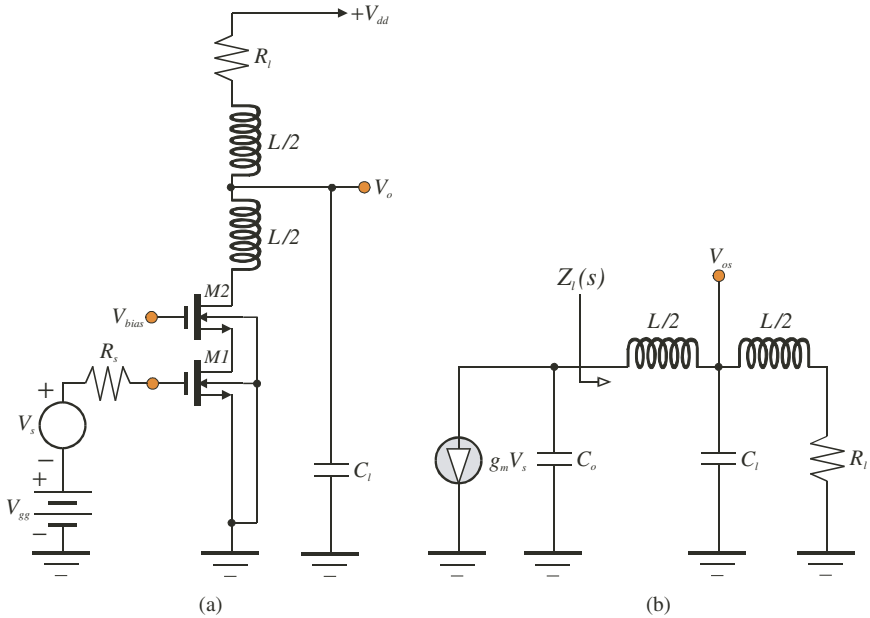


Figure 9.23. (a) Schematic diagram of a series-shunt peaked amplifier driving a capacitive load. (b) Approximate small signal model of the amplifier in (a). As usual, the transistors are biased in their saturation regimes.

capacitance, C_i . The $L/2$ inductance incident with the drain terminal of the cascode transistor, $M2$, serves as a series peaking element, while the inductance in series with resistance R_l functions as the shunt peaking element. Fig. 9.23(b) is the corresponding small signal model, which reflects the recurring themes of large transistor channel resistances, negligible bulk-induced modulation of threshold voltage, and an effective output capacitance, C_o , which is nominally the sum of the bulk-drain and gate-drain capacitances of transistor $M2$.

9.6.1. Design Criteria

In principle, it is possible to deduce the transfer function, V_{os}/V_s , for the model in Fig. 9.23(b), but the fourth order nature of the circuit renders a useful quantification of bandwidth enhancement a daunting analytical ordeal. A more pragmatic tack derives from the observation that the model at hand is the topology of a lumped approximation to a distributed transmission line.^{[5]–[7]} In particular, it is possible to choose the drain load resistance,

R_l , in a manner that renders $Z_l(s)$ equal to R_l , independent of indicated inductances and capacitances, over a broad range of signal frequencies. The advantage of constant $Z_l(s)$ is a simplification of the pertinent transfer function and hence, a presumably tractable and designable bandwidth relationship.

An inspection of the model in Fig. 9.23(b) reveals

$$Z_l(s) = \frac{sL}{2} + \frac{R_l + \frac{sL}{2}}{1 + sR_lC_l + \frac{s^2LC_l}{2}}. \quad (9-76)$$

It is a straightforward matter to show that $Z_l(s) \equiv R_l$ if R_l is selected to satisfy

$$R_l = \sqrt{\left(\frac{L}{C_l}\right) \left[1 + \left(\frac{s}{\omega_h}\right)^2\right]}, \quad (9-77)$$

where

$$\omega_h = \frac{2}{\sqrt{LC_l}}. \quad (9-78)$$

Obviously, a frequency dependent, passive resistance of the form propounded by Eq. (9-77) is physically unrealizable. But if the frequency parameter, ω_h , is suitably large in comparison to the outer reach of the amplifier passband,

$$R_l \approx \sqrt{\frac{L}{C_l}} \quad (9-79)$$

is very much realizable, whereupon

$$\omega_h = \frac{2}{\sqrt{LC_l}} \approx \frac{2}{R_lC_l}. \quad (9-80)$$

Armed with the preceding two expressions and the tacit (and not completely satisfying) presumption that capacitance C_o can be ignored in the model of Fig. 9.23(b), the applicable transfer function can be shown to be

$$A_v(s) = \frac{V_{os}}{V_s} \approx -\frac{g_m R_l \left(1 + \frac{s}{\omega_h}\right)}{1 + 2\left(\frac{s}{\omega_h}\right) + 2\left(\frac{s}{\omega_h}\right)^2}. \quad (9-81)$$

Following straightforward analytical procedures invoked previously, the compensated 3-dB bandwidth, B_c , can be shown to be

$$B_c = 0.8995\omega_h = \frac{1.80}{R_l C_l}, \quad (9-82)$$

where Eq. (9-80) is used. If capacitance C_o is indeed negligible, the inverse of the time constant, $R_l C_l$, is the amplifier bandwidth prior to series-shunt peaked compensation and thus, Eq. (9-82) suggests an outstanding 80% improvement in bandwidth. This upgraded performance comes with a slight price, which can be shown to be 2.91% of magnitude response peaking occurring at a frequency of $0.687/R_l C_l$.

9.6.2. A Design Problem

Although the tacit neglect of the amplifier output capacitance, C_o , encourages a tractably straightforward frequency response analysis of the series-shunt peaked amplifier in Fig. 9.23, such neglect also obscures a potentially catastrophic design problem. In an attempt to dramatize the nature of this problem, assume that the amplifier in question utilizes the transistors exploited in Example 9.2 and is to be designed for a voltage gain of 15 dB and a 3-dB bandwidth of 3 GHz. From Eq. (9-82), the required value of ω_h is $2\pi(3.335 \text{ GHz})$. Since 15 dB is a gain magnitude of 5.623, $g_m = 34 \text{ mmho}$ yields a required drain circuit load resistance of $R_l = 165.4 \Omega$. It follows from Eq. (9-80) that the load capacitance delivering the stipulated bandwidth must be $C_l = 577.0 \text{ fF}$. Finally, Eq. (9-79) yields $L = 15.78 \text{ nH}$, whence $L/2 = 7.89 \text{ nH}$.

The HSPICE simulation of the magnitude response of the model in Fig. 9.23(b), given the foregoing computed parameters and the presumption that $C_o = 0$, is depicted in Fig. 9.24. The simulated 3-dB bandwidth is 3.0 GHz, which is precisely the bandwidth objective. Moreover, the simulated maximum value of the magnitude response is 5.787, or 2.86% of peaking, which doubtlessly differs from the theoretic percentage peaking of 2.91% only because of restrictions implicit to the quantized frequency scale adopted for the circuit simulation. On the other hand, Fig. 9.25 compares the foregoing $C_o = 0$ simulation of the magnitude response to its $C_o = 27 \text{ fF}$ (the sum of C_{gd} and C_{bd} for transistor $M2$) counterpart. Despite the close match between the two simulated frequency responses for frequencies extending through the 3-dB bandwidth, even the most sedentary

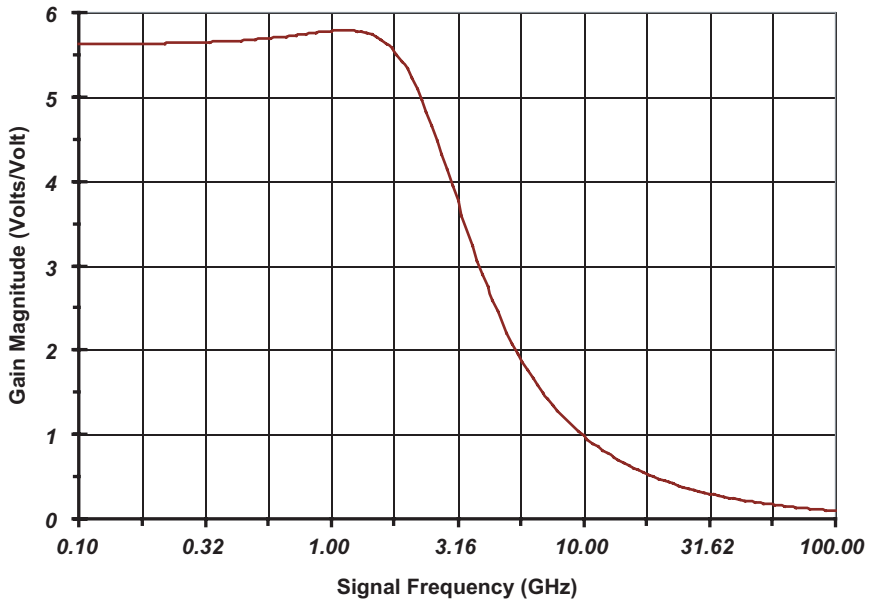


Figure 9.24. Magnitude response of the series-shunt peaked amplifier modeled in Fig. 9.23(b). The model parameters are $g_m = 34$ mmho, $L/2 = 7.89$ nH, $C_l = 577$ fF, $R_l = 165.4$ Ω , and notably, $C_o = 0$.

of circuit designers is likely to become hypertensive at the sight of the apparent resonance, in this case at 10.96 GHz.

The cause of the indicated resonance in the $C_o = 27$ fF response curve depicted in Fig. 9.25 is somewhat transparent. In particular, at high signal frequencies, the relatively large load capacitance, C_l , begins to emulate a signal short circuit. At these frequencies, the inductance, $L/2$, to the left of capacitance C_l in Fig. 9.23(b) is resultantly placed in virtual shunt with the amplifier output port capacitance, C_o . It follows that the observed resonant frequency derives from the effective shunt interconnection of these two elements, whence, the radial resonant frequency, say ω_o , is

$$\omega_o \approx \frac{1}{\sqrt{(L/2) C_o}} = 2\pi(10.90 \text{ GHz}). \quad (9-83)$$

In order to mitigate the foregoing dilemma, steps must be taken to ensure that the parasitic output capacitance, C_o , of the transconductor cell does not face an inductive impedance, $Z_l(s)$, seen looking into the tee configuration

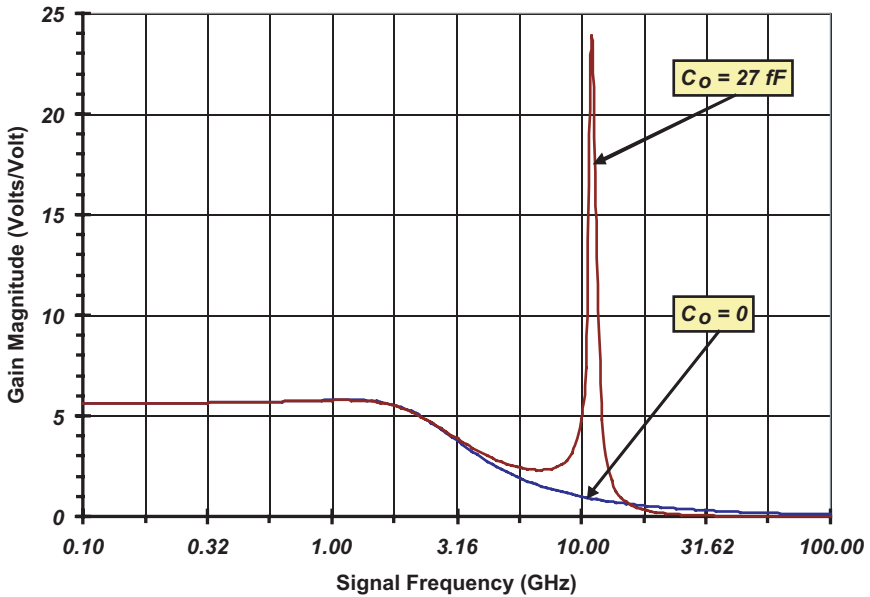


Figure 9.25. Magnitude responses of the series-shunt peaked amplifier modeled in Fig. 9.23(b). The model parameters are identical to those that underlie the simulated response drawn in Fig. 9.24, except for the indicated differences in the amplifier output port capacitance, C_o .

comprised of the two inductances, $L/2$, and the load capacitance, C_l , in Fig. 9.23(b). Since a capacitive tee input impedance is also undesirable because it foretells a possible degradation in circuit 3-dB bandwidth, it follows that a constant, frequency invariant $Z_l(s)$ is a necessary condition for design optimality in the senses of broadbanded and reasonably flat frequency responses. In other words, the subject tee network must be modified so that the frequency dependent $Z_l(s)$ that results from approximating the load requirement of Eq. (9-77) by Eq. (9-79) becomes frequency invariant for a stipulated drain load resistance, R_l .

9.6.2.1. Capacitance Bridged, Coupled Inductor Load

An intriguing broadband circuit architecture satisfying the foregoing design requirements is the circuit shown in Fig. 9.26.^[8] This configuration, which is an outgrowth of classic shunt and double series peaking strategies, modifies the circuit of Fig. 9.23(a) by appending a bridging capacitance, C_f , across the two symmetrical coils in the hope that this element can mitigate

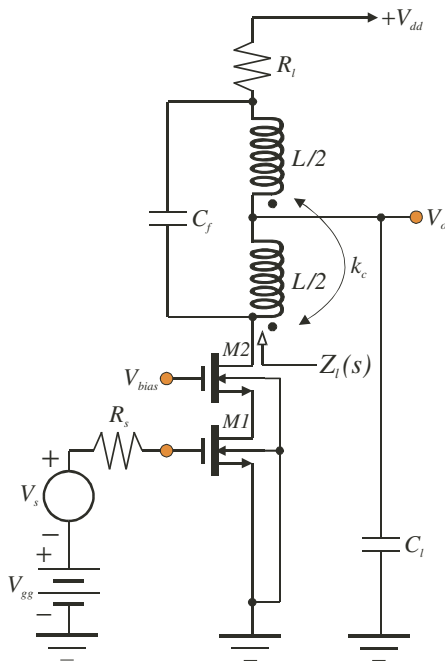


Figure 9.26. Modified version of the broadband peaking circuit in Fig. 9.23(a). Observe the use of magnetically coupled inductors and the incorporation of a bridging capacitance across the tee circuit.

the inductive component of the tee input impedance without appreciable bandwidth degradation. The mere fact that C_f can be selected to achieve a purely resistive $Z_i(s)$ does not necessarily guarantee an acceptably flat frequency response for the small signal voltage gain function, V_{os}/V_s . To this end, an additional design degree of freedom is forged by purposefully laying out the two coils to incur a presumably controllable mutual inductance, M . This mutual inductance is characterized classically by the so-called coupling coefficient, k_c , between the two coils, such that

$$k_c = \frac{M}{L/2}. \tag{9-84}$$

For $k_c = 0$, the inductors operate independently of one another (meaning that the electromagnetic fields surrounding one inductor do not envelope any portion of the coils implicit to the other inductor), while for $k_c = 1$, the inductors are maximally coupled, as in an ideal transformer. In silicon

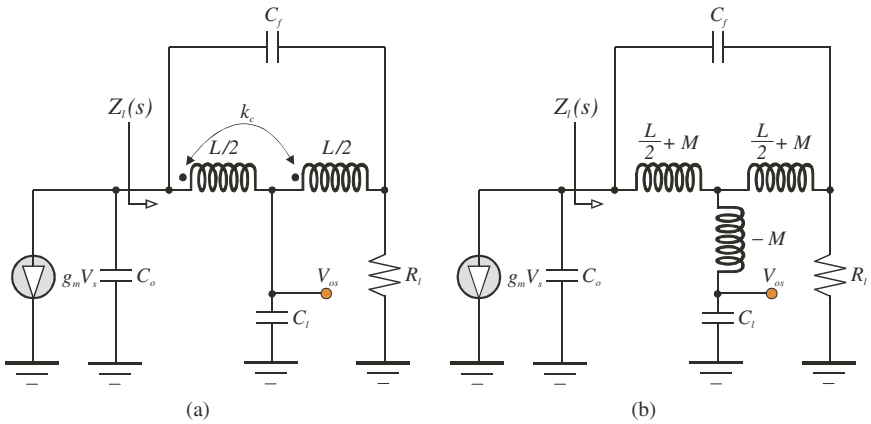


Figure 9.27. (a) Small signal, high frequency equivalent circuit of the broadband amplifier shown in Fig. 9.26. (b) Alternative form of the model in (a).

integrated circuits, spiral inductors can be laid out to yield coupling coefficients in the range of $k_c \leq 0.5$. On the other hand proximately located bond wires can be positioned to achieve inductive coupling coefficients of $k_c \leq 0.7$.

The small signal, high frequency model of the amplifier in Fig. 9.26 is provided in Fig. 9.27(a). In order to facilitate circuit analysis, and as the reader is invited to demonstrate in Problem 9.9 at the conclusion of this chapter, the two coupled inductances can be represented electrically as the uncoupled tee inductor two-port network drawn in Fig. 9.27(b). It is interesting to note that the second model suggests that the immediate effect of inductive coupling is to incur additional series peaking of the circuit load capacitance, C_l , thereby arguably leading to the possibility of improving the bandwidth established by conventional series-shunt peaking.

9.6.2.2. Constant Resistance Criteria

In order to arrive at the criteria ensuring constant $Z_l(s)$, and in particular, $Z_l(s) \equiv R_l$ for all signal frequencies, it is expedient to view the load network in Fig. 9.27(b) as a shunt interconnection of the bridging capacitance, C_f , and the inductive tee network, as is exemplified in Fig. 9.28. Such a view promotes the notion that the short circuit admittance, or y-parameters, of the overall network are the sum of the corresponding y-parameters of each of the two networks. To this end, the short circuit input admittance, y_{11a} , of

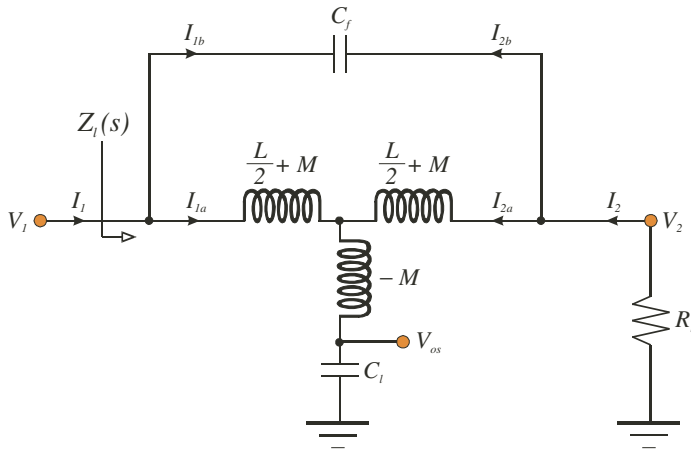


Figure 9.28. The load circuit in Fig. 9.27(b) drawn to underscore the fact that the structure is a shunt-shunt interconnection of two linear two-port networks.

the inductive tee configuration is

$$y_{11a} = \left. \frac{I_{1a}}{V_1} \right|_{V_2=0} = \frac{1 + \frac{s^2 LC_l}{2}}{s(1 + k_c) L \left[1 + \frac{s^2 (1 - k_c) LC_l}{4} \right]}, \quad (9-85)$$

where Eq. (9-84) has been used. The transadmittance, y_{12a} , can be shown to be

$$y_{12a} = \left. \frac{I_{1a}}{V_2} \right|_{V_1=0} = - \frac{1 - \frac{s^2 k_c LC_l}{2}}{s(1 + k_c) L \left[1 + \frac{s^2 (1 - k_c) LC_l}{4} \right]}. \quad (9-86)$$

Because of the symmetrical nature of the passive network at hand,

$$\left. \begin{aligned} y_{11a} = \left. \frac{I_{1a}}{V_1} \right|_{V_2=0} &\equiv y_{22a} = \left. \frac{I_{2a}}{V_2} \right|_{V_1=0} \\ y_{12a} = \left. \frac{I_{1a}}{V_2} \right|_{V_1=0} &\equiv y_{21a} = \left. \frac{I_{2a}}{V_1} \right|_{V_2=0} \end{aligned} \right\}. \quad (9-87)$$

For the bridging capacitance two port, it is obvious that

$$y_{11b} = \left. \frac{I_{1b}}{V_1} \right|_{V_2=0} = sC_f \equiv \left. \frac{I_{2b}}{V_2} \right|_{V_1=0} = y_{22b}, \quad (9-87)$$

and

$$y_{12b} = \left. \frac{I_{1b}}{V_2} \right|_{V_1=0} = -sC_f \equiv \left. \frac{I_{2b}}{V_1} \right|_{V_2=0} = y_{21b}. \quad (9-88)$$

It follows that the overall network is characterized by the y -parameter functions,

$$y_{11} \equiv y_{22} = y_{11a} + y_{11b} = \frac{1 + \frac{s^2 LC_l}{2}}{s(1+k_c)L \left[1 + \frac{s^2(1-k_c)LC_l}{4} \right]} + sC_f, \quad (9-89)$$

and

$$\begin{aligned} y_{12} \equiv y_{21} &= y_{12a} + y_{12b} \\ &= -\frac{1 - \frac{s^2 k_c LC_l}{2}}{s(1+k_c)L \left[1 + \frac{s^2(1-k_c)LC_l}{4} \right]} - sC_f, \end{aligned} \quad (9-90)$$

A review of Sections 2.3.3 and 2.4.3 of this text confirms that the driving point impedance, $Z_l(s)$, highlighted in Fig. 9.28 derives from the expression,

$$\frac{1}{Z_l(s)} = y_{11} - \frac{y_{12}^2}{y_{11} + \frac{1}{R_l}}. \quad (9-91)$$

Since $Z_l(s) \equiv R_l$ is the design objective, Eq. (9-91) gives rise to the constraint,

$$\frac{1}{R_l} = \sqrt{(y_{11} + y_{12})(y_{11} - y_{12})}. \quad (9-92)$$

Upon substitution of Eqs. (9-89) and (9-90) into Eq. (9-92),

$$\frac{1}{R_l} = \sqrt{\frac{C_l}{(1+k_c)L} \left[\frac{1 + s^2(1+k_c)LC_f}{1 + \frac{s^2(1-k_c)LC_l}{4}} \right]}. \quad (9-93)$$

Within the radical on the right hand side of this expression, note the presence of conjugate imaginary zero and pole pairs. If capacitance C_f is chosen as

$$C_f = \frac{C_l}{4} \left(\frac{1-k_c}{1+k_c} \right), \quad (9-94)$$

the aforementioned imaginary zeros and poles cancel, thereby producing the frequency independent expression,

$$\frac{1}{R_l} = \sqrt{\frac{C_l}{(1 + k_c)L}}, \quad (9-95)$$

for the resistive load termination, R_l , that produces a driving point input impedance that is identical to said load resistance. For a given value of R_l , Eq. (9-95) stipulates a requisite inductance, L , of

$$L = \frac{R_l^2 C_l}{1 + k_c}. \quad (9-96)$$

Equations (9-94) and (9-96) comprise necessary and sufficient conditions underlying the realization of an input impedance, $Z_l(s)$, that is purely resistive and equal to the load resistance, R_l , for all signal frequencies. Note that this constant resistance characteristic can be achieved even when the two utilized inductors are uncoupled; that is, when $k_c = 0$. When the inductors are perfectly coupled in the sense of $k_c = 1$, Eq. (9-94) shows that no bridging capacitance is required for constant input resistance behavior of the network at hand.

9.6.2.3. Transfer Relationship

Armed with Eqs. (9-94) and (9-96), the small signal voltage transfer function, $A_v(s) = V_{os}/V_s$, can be cast, albeit somewhat painfully, in a useful closed form format. This analysis is also facilitated by the design constraint, $Z_l(s) \equiv R_l$ in Fig. 9.27(b), which implies that the time constant associated with the transconductor output capacitance, C_o , is simply $R_l C_o$. If the inverse of this time constant is significantly larger than the desired, compensated radial bandwidth, B_c , so that $B_c R_l C_o \ll 1$, capacitance C_o can be ignored tacitly to garner a modicum of simplified circuit analysis. Then, applying the same gain normalization as that introduced in Eq. (9-65), the normalized transfer relationship that derives because of Eqs. (9-94) and (9-96) is

$$A_n(s) = \frac{1}{1 + \frac{s}{Q_c \omega_x} + \left(\frac{s}{\omega_x}\right)^2}, \quad (9-97)$$

where the quality factor, Q_c , is

$$Q_c = \sqrt{\frac{1 - k_c}{1 + k_c}}, \quad (9-98)$$

and the frequency parameter, ω_x , is given by

$$\omega_x = \frac{2}{\sqrt{LC_l(1-k_c)}} = \frac{2}{Q_c R_l C_l}, \quad (9-99)$$

where Eqs. (9-96) and (9-98) have been exploited. Since the uncompensated bandwidth, B_{cs} , indigenous to $L = M = 0$ and $C_f = 0$ is approximately the inverse of the time constant, $R_l(C_o + C_l)$, observe that ω_x in Eq. (9-99) is also expressible as

$$\omega_x = \frac{2}{\sqrt{LC_l(1-k_c)}} = \frac{2}{Q_c R_l C_l} \approx \frac{2B_{cs}}{Q_c} \left(1 + \frac{C_o}{C_l}\right). \quad (9-100)$$

A comparison of Eq. (9-97) with Eq. (9-66) suggests that if quality factor Q_c is set to the inverse of root two, the peaking circuit at hand delivers a second order, Butterworth, maximally flat magnitude frequency response whose radial 3-dB bandwidth is precisely ω_x . From Eq. (9-98), $Q_c = 1/\sqrt{2}$ is tantamount to the requirement, $k_c = 1/3$, which lies well within the coupling coefficient domain of monolithic inductor pairs. For this design constraint, note from Eq. (9-100) that the resultant bandwidth, B_c , of the compensated structure, optimized for maximally flat magnitude response, is

$$\omega_x = B_c \approx 2\sqrt{2} \left(1 + \frac{C_o}{C_l}\right) B_{cs}, \quad (9-101)$$

which suggests an impressive bandwidth enhancement factor approaching three.

It is important to stress that ω_x is the 3-dB bandwidth of the network represented by the transfer function in Eq. (9-97) if and only if Q_c is chosen to achieve a maximally flat magnitude response. In general, the compensated bandwidth, B_c , can be determined by studying the network at hand for steady state sinusoidal signal excitation, wherein the applicable transfer relationship is

$$A_n(j\omega) = \frac{1}{1 + \frac{j\omega}{Q_c \omega_x} - \left(\frac{\omega}{\omega_x}\right)^2}. \quad (9-102)$$

Accordingly, bandwidth B_c derives from

$$\left[1 - \left(\frac{B_c}{\omega_x}\right)^2\right]^2 + \left(\frac{B_c}{Q_c \omega_x}\right)^2 = 2, \quad (9-103)$$

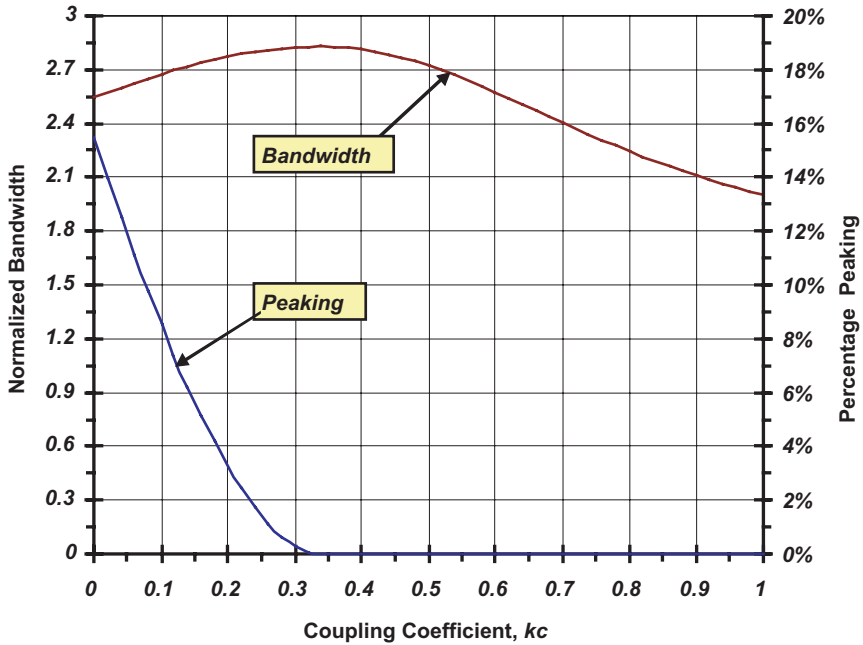


Figure 9.29. The normalized bandwidth and the percentage of magnitude response peaking for the broadbanded amplifier modeled in Fig. 9.27. The bandwidth curve is normalized to the uncompensated bandwidth, B_{cs} , of the amplifier and exploits the presumption of a transconductor output capacitance much smaller than the load capacitance driven by the amplifier.

whose solution, using Eq. (9-100), can be shown to be

$$\frac{B_c}{B_{cs}} = \left(1 + \frac{C_o}{C_l}\right) \frac{2}{Q_c} \sqrt{\sqrt{\left[\left(\frac{1}{2Q_c^2} - 1\right)^2 + 1\right]} - \left(\frac{1}{2Q_c^2} - 1\right)} \tag{9-104}$$

Of course, this normalized bandwidth can be expressed explicitly in terms of the inductor coupling coefficient, k_c , by combining Eq. (9-98) with Eq. (9-104). To this end, Fig. 9.29 graphically depicts the dependence of the normalized bandwidth on the coupling coefficient for the case in which the transconductor output capacitance, C_o , is much smaller than the load capacitance, C_l . Observe that $k_c = 1/3$, which corresponds to $Q_c = 1/\sqrt{2}$, produces a bandwidth that, in addition to agreeing with Eq. (9-101), is the

maximum achievable bandwidth of the subject network. Even more interesting, as well as appealing from an integrated circuit design and layout perspective, is the observation that the normalized bandwidth is not a particularly sensitive function of the coupling coefficient, whose precise numerical value is vulnerable to routinely encountered process vagaries and parametric uncertainties. For example, over the coefficient range, $0.1 \leq k_c \leq 0.5$, B_c/B_{cs} varies from only 2.67 to its peak of 2.82.

Although B_c/B_{cs} is not a sensitive function of k_c , a magnitude response peaking penalty is paid when $k_c \neq 1/3$. The frequency, say ω_p , at which the magnitude response is maximized can be deduced by equating the frequency derivative of the magnitude function in Eq. (9-102) to zero. The result is

$$\omega_p = \omega_x \sqrt{1 - \frac{1}{2Q_c^2}}. \quad (9-105)$$

Since ω_p is an imaginary number for $Q_c < 1/\sqrt{2}$, response peaking is manifested if and only if $Q_c > 1/\sqrt{2}$, or equivalently, for $k_c < 1/3$. Note further that for $Q_c = 1/\sqrt{2}$, $\omega_p = 0$, which suggests that the peak value of the transfer function occurs only at zero frequency, which is as it should be in a lowpass, maximally flat magnitude network. It is a simple matter to show that the actual magnitude peak, say M_p , corresponding to $\omega = \omega_p$ is

$$M_p = \frac{Q_c}{\sqrt{1 - \frac{1}{4Q_c^2}}}. \quad (9-106)$$

It is to be understood that in concert with the disclosures underpinning Eq. (9-105), Eq. (9-106) is valid only for $k_c \leq 1/3$; otherwise, $M_p = 1$. Superimposed with the normalized bandwidth curve in Fig. 9.29 is a plot of the percentage by which the magnitude response peak, M_p , exceeds the zero frequency, unity gain value of the network transfer characteristic. This percentage peaking is somewhat sensitive to k_c but nonetheless, the maximum observable peaking, which occurs for the uncoupled inductor case evidenced by $k_c = 0$, is only about 15.5%.

Example 9.5. When driven by a 50Ω signal source, the amplifier in Fig. 9.26 is to be designed to deliver a maximally flat response characterized by a zero frequency voltage gain of 16 dB and a 3-dB frequency of 10 GHz. The utilized transistor is the same as the device exploited in Example 9.3. Design the circuit by determining the appropriate values of the coupled inductances, the coupling coefficient, k_c , of the inductors, the drain load resistance, R_l , the requisite load capacitance, C_l , and the bridging capacitance, C_f , required at the amplifier output port. Using the

small signal model in Fig. 9.27(a), simulate the small signal frequency response, V_{os}/V_s , of the finalized design on HSPICE. Compare the frequency response of the compensated amplifier with that of its uncompensated counterpart.

Solution 9.5.

- (1) A voltage gain of 16 dB is equivalent to a numerical gain of 6.310. In a cascode arrangement of a common source amplifier, the effects of drain-source channel resistance are entirely negligible. Thus, the voltage gain magnitude is $g_m R_l$, whence a required drain load resistance of $R_l = 185.6 \Omega$.
- (2) Since the uncompensated common source amplifier bandwidth is $B_{cs} = 1/R_l(C_o + C_l)$, Eq. (9-101) yields

$$B_c = \frac{2\sqrt{2}}{R_l C_l}. \quad (\text{E5-1})$$

With $B_c = 2\pi(10 \text{ GHz})$ and $R_l = 185.6 \Omega$, the required load capacitance is seen to be $C_l = 242.6 \text{ fF}$. The net output capacitance, C_o , of the transconductor driver is the sum, $(C_{gd} + C_{bd})$, of gate-drain and bulk-drain capacitances of the cascode transistor, $M2$, in the circuit of Fig. 9.26. Since $C_o = C_{gd} + C_{bd} = 27 \text{ fF}$ is only about nine times smaller than the required value of load capacitance C_l , and since C_o is tacitly ignored in all analyses executed on the broadband configuration, engineering prudence dictates a reduction of the computed value of C_l by nominally five percent. Accordingly, and in the hope of mitigating the deleterious consequences of an output port capacitance, C_o , that is not entirely negligible in comparison to the load capacitance, select $C_l = 230 \text{ fF}$.

- (3) The required coupling coefficient for a Butterworth, maximally flat magnitude response is $k_c = 1/3$. Using Eq. (9-96) with $R_l = 185.6 \Omega$ and $C_l = 230 \text{ fF}$, the requisite half inductance value is $L/2 = 2.970 \text{ nH}$.
- (4) From Eq. (9-94), the bridging capacitance with $C_l = 230 \text{ fF}$ and $k_c = 1/3$ is $C_f = 28.75 \text{ fF}$.
- (5) Figure 9.30 depicts the small signal models for both the uncompensated and the compensated cascode amplifiers. The simulated magnitude responses of both of these structures appear in Fig. 9.31. Observe that both responses are flat over the frequency passband of interest.

Comments. An assiduous inspection of the HSPICE simulation results reveals a 3-dB bandwidth for the compensated amplifier of 10.02 GHz, which clearly satisfies the bandwidth design target. On the other hand, the uncompensated unit shows a bandwidth of 3.33 GHz, which, as previously conjectured, is less than the bandwidth of the compensated cell by a factor of nominally three-fold.

By any engineering measure, the bandwidth compensation strategy entailing a bridging capacitance in shunt with two coupled inductances comprises a satisfying broadbanding methodology. To be sure, a verification of the broadbanding scheme

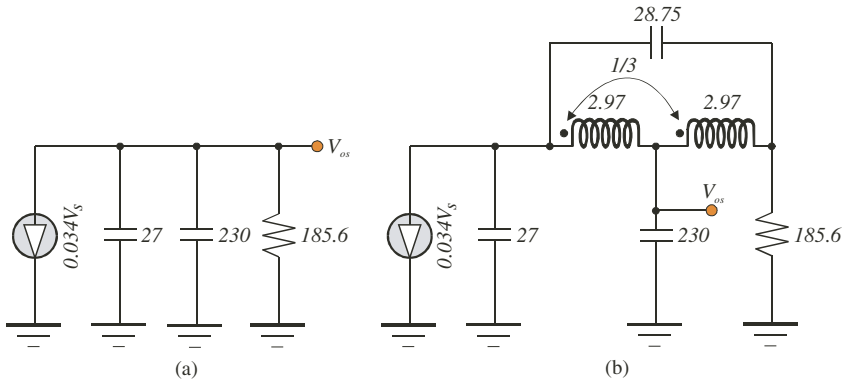


Figure 9.30. (a) Small signal model of the uncompensated amplifier addressed in Example 9.5. (b) Small signal model of the compensated amplifier designed for maximally flat magnitude response in Example 9.5. All capacitance values are in femtofarads, resistances are in units of ohms, and inductance values are in units of nanohenries.

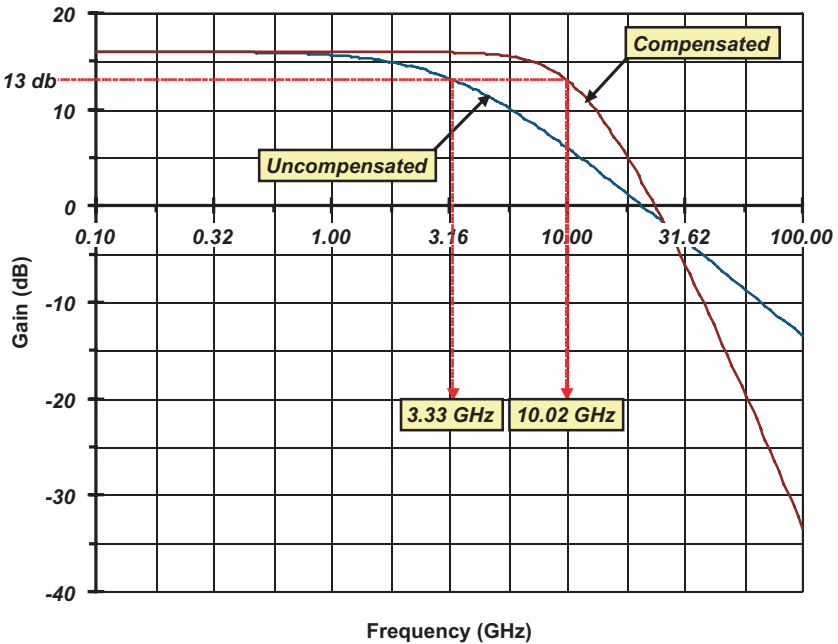


Figure 9.31. Frequency responses of the amplifiers addressed in Example 9.5. The “uncompensated” curve pertains to the small signal model in Fig. 9.30(a), while the “compensated” curve refers to the model of Fig. 9.30(b).

is provided by means of small signal analyses and simulations executed on only pertinent small signal models. This verification procedure is defensible from two points of view. First, the purpose of this textbook is not electronic circuit and system analysis and design. Instead, a principle purpose of this text is to demonstrate that the insightful engineering understanding deriving from an application of classic circuit theoretic tools and mathematically sound circuit analyses conduces innovative circuit design solutions. Second, it should be understood that the ability to glean acceptable responses in a relevant small signal model is a necessary condition for achieving satisfactory performance in the electronic amplifier ultimately configured for integrated circuit layout and processing.

9.7.0. Broadbanding via Feedback

The preceding sections of material underscore open loop broadbanding methods, wherein transmission zeros are introduced to mitigate the deleterious effects exerted on open loop bandwidth by dominant network poles. As alluded to in the introductory section of this chapter, negative feedback constitutes a viable alternative to open loop broadbanding, provided that problems surrounding potentially underdamped open loop responses are circumvented without incurring substantive penalties on achievable closed loop bandwidth. To this end, the dual loop, shunt-series feedback amplifier, whose basic schematic form is the structure in Fig. 9.32(a), is a commonly used broadband topology. In this amplifier, for which the approximate high frequency model is the diagram of Fig. 9.32(b), R_s represents the Thévenin signal source resistance, R_l is the load resistance driven by the circuit, while resistances R_i and R_o are incorporated for biasing purposes. The resistance, R_{ss} , establishes series feedback around the open loop, while resistance R_f realizes shunt feedback. The small signal equivalent circuit in Fig. 9.32(b) tacitly ignores the channel resistance and bulk-induced threshold modulation in the transistor. Moreover, C_{gs} and C_{gd} are the traditional gate-source and gate-drain capacitances of the MOSFET, while capacitance C_l accounts for the bulk-drain capacitance of the transistor, as well as for any load capacitance associated with the terminated output port.

Compared with the open loop topologies studied earlier, the advantages of the feedback amplifier in Fig. 9.32(a) include improved linearity and diminished sensitivity of forward gain with respect to active element parameters. Additionally, its dual loop nature provides controllable and predictable driving point input and output impedances, Z_{in} and Z_{out} , at least for signal frequencies lying within the amplifier passband. A clue as to the controllable nature of Z_{in} and Z_{out} derives from observing that if resistance

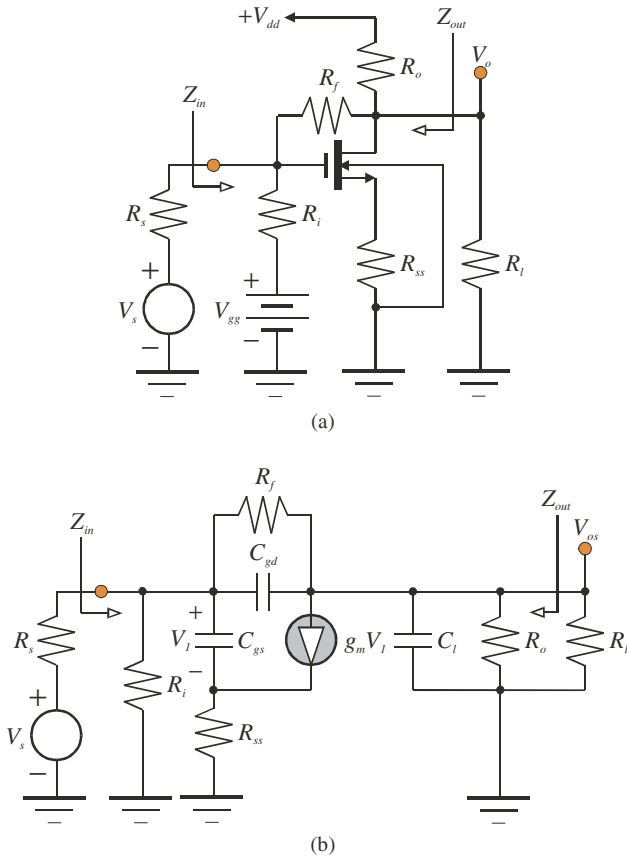


Figure 9.32. (a) Basic schematic diagram of a shunt-series feedback amplifier. The transistor is biased in saturation. (b) Approximate small signal, high frequency model of the amplifier in (a).

R_f is supplanted by an open circuit, the feedback resistance, R_{ss} , confers a transadmittance amplifier featuring extremely high driving point input and output impedances. On the other hand, a short circuited R_{ss} leaves feedback resistance R_f to forge a transimpedance amplifier characterized by very low input and output impedances. It is therefore reasonable to surmise the likelihood that the presence of both R_{ss} and R_f , which is tantamount to coalescing transadmittance operation with transimpedance signal processing, leads to finite and predictable Z_{in} and Z_{out} . The analyses that follow confirm the propriety of this expectation. Indeed, Z_{in} and Z_{out} are not only predictable,

their low frequency constituents, R_{in} and R_{out} , respectively, can be equated if the source resistance, R_s , is matched to the load resistance, R_l . Moreover, it is possible to realize the subject dual loop amplifier in such a way that it delivers the so-called *match terminated* case of $R_s = R_{in} = R_{out} = R_l$. At least three engineering attributes accompany the match terminated circumstance. First, a cascade of stages of the form depicted in Fig. 9.32(a) can be implemented without the interstage loading effects that cause gain attenuation and even outright uncertainty in the cascaded value of gain. Second, maximum power transfer is engaged between the output port of an amplifier and the amplifier input port to which said output port is incident. Finally, if $R_s = R_l$ is a relatively small resistance ($50\ \Omega$ or less), bandwidth degradation owing to parasitic *I/O* port capacitances is minimal. To the latter end, the achievable 3-dB bandwidth is more limited by active device characteristics and in particular, the unity gain frequency of the transistor, than it is by parasitic capacitances at either the source or load ports.

9.7.1. Low Frequency Characteristics

The low frequency version of the small signal model shown in Fig. 9.32(b) is given in Fig. 9.33(a). Using signal flow analyses, the low frequency voltage gain, A_{vo} , of the shunt-series feedback amplifier is expressible as

$$A_{vo} = \frac{V_{os}}{V_s} = A_{os} \left[\frac{1 + R_{To}(R_s, R_l)/R_f}{1 + R_T(R_s, R_l)/R_f} \right], \quad (9-107)$$

where A_{os} is the null parameter voltage gain evaluated under the condition that the conductance, say G_f , associated with feedback resistance R_f is set to zero. The function, $R_T(R_s, R_l)$, is the normalized return ratio with respect to conductance G_f , while $R_{To}(R_s, R_l)$ is the normalized null return ratio with respect to G_f . On the other hand, the driving point input resistance, R_{in} , is expressible as

$$R_{in} = R_{ino} \left[\frac{1 + R_T(0, R_l)/R_f}{1 + R_T(\infty, R_l)/R_f} \right], \quad (9-108)$$

while the driving point output resistance, R_{out} , is given by

$$R_{out} = R_{outo} \left[\frac{1 + R_T(R_s, 0)/R_f}{1 + R_T(R_s, \infty)/R_f} \right]. \quad (9-109)$$

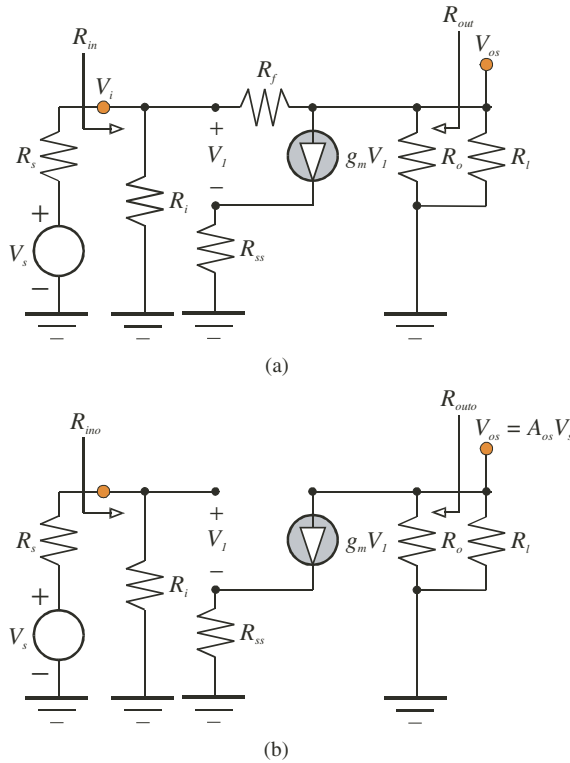


Figure 9.33. (a) Approximate low frequency model of the shunt-series feedback amplifier in Fig. 9.32(a). (b) Amplifier model appropriate for the evaluation of the low frequency values of the open loop voltage gain, A_{os} , the driving point input resistance, R_{ino} , and the driving point output resistance, R_{outo} , for the null feedback parameter case of $1/R_f = 0$.

Figure 9.33(b) is the model in Fig. 9.33(a), with resistance R_f open circuited; that is, the model at hand is pertinent to an open loop, with respect to the shunt-shunt feedback element, at low frequency operating conditions. An inspection of this model reveals

$$A_{os} = \left. \frac{V_{os}}{V_s} \right|_{R_f=\infty} = -g_{me} \left(\frac{R_i}{R_i + R_s} \right) (R_o \parallel R_L), \quad (9-110)$$

where the effective forward transconductance, g_{me} , of the amplifier is

$$g_{me} = \frac{g_m}{1 + g_m R_{ss}}. \quad (9-111)$$

A further inspection of the model at hand shows that the input resistance, R_{ino} , under the condition of $R_f = \infty$, is

$$R_{ino} = R_i, \tag{9-112}$$

and the corresponding null feedback parameter output resistance, R_{outo} , is

$$R_{outo} = R_o. \tag{9-113}$$

The equivalent circuit relative to the computation of the normalized return ratio, $R_T(R_s, R_l)$, appears in Fig. 9.34(a), while the normalized null return ratio, $R_{T_o}(R_s, R_l)$, derives from an analysis of the structure shown in Fig. 9.34(b). It is a straightforward task to show that in Fig. 9.34(a),

$$R_T(R_s, R_l) = \left. \frac{V_x}{I_x} \right|_{V_s=0} = (R_o \parallel R_l) + [1 + g_{me}(R_o \parallel R_l)] (R_i \parallel R_s). \tag{9-114}$$

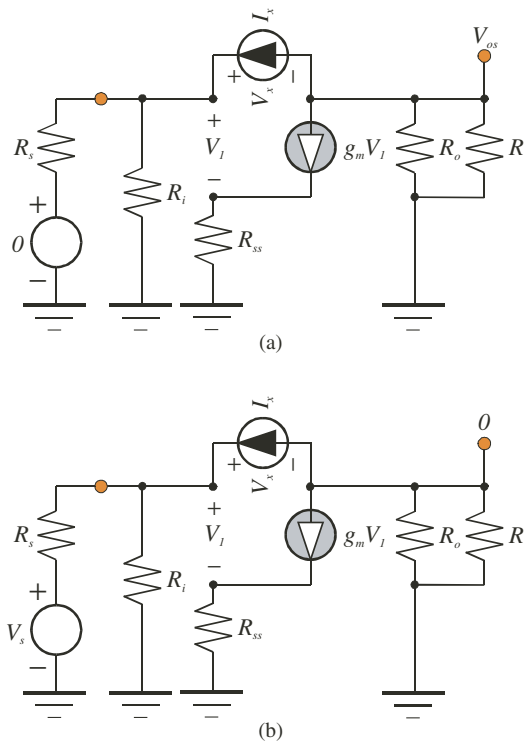


Figure 9.34. (a) Low frequency model of the shunt-series feedback amplifier used in the computation of the normalized return ratio, $R_T(R_s, R_l)$. (b) Low frequency model exploited to compute the null normalized return ratio, $R_{T_o}(R_s, R_l)$.

On the other hand, Fig. 9.34(b) confirms

$$R_{To}(R_s, R_l) = \left. \frac{V_x}{I_x} \right|_{V_{os}=0} = -\frac{1}{g_m} \left[1 + (1 + g_m R_i) \left(\frac{R_{ss}}{R_i} \right) \right]. \quad (9-115)$$

If Eqs. (9-114) and (9-112) are combined with Eq. (9-108), the driving point input resistance is found to be

$$R_{in} = R_i \left\| \left[\frac{R_f + (R_o \parallel R_l)}{1 + g_{me}(R_o \parallel R_l)} \right] \right. \quad (9-116)$$

For the output resistance, Eqs. (9-114), (9-113), and (9-109) coalesce to deliver

$$R_{out} = R_o \left\| \left[\frac{R_f + (R_i \parallel R_s)}{1 + g_{me}(R_i \parallel R_s)} \right] \right. \quad (9-117)$$

It is interesting to note that if $R_i = R_o$ and $R_s = R_l$, $R_{in} \equiv R_{out}$. If $R_s = R_l \triangleq R$, the match terminated constraint of $R_s = R_l = R_{in} = R_{out} \equiv R$ requires

$$R_f = [1 + g_{me}(R_i \parallel R)] \left(\frac{R_i R}{R_i - R} \right) - (R_i \parallel R). \quad (9-118)$$

Since resistance R must be small to support broadband design objectives, resistances R_i and R_o can be chosen to ensure that both R_i and R_o are significantly larger than R . Under this design guideline, Eq. (9-118) collapses to the requirement,

$$R_f \approx g_{me} R^2 = \frac{g_m R^2}{1 + g_m R_{ss}}. \quad (9-119)$$

A determination of the low frequency closed loop gain corresponding to the foregoing match terminated condition requires the substitution of Eqs. (9-110), (9-114), and (9-115) into Eq. (9-107). In view of Eq. (9-119) and its underlying approximations, this voltage gain is

$$\begin{aligned} A_{vo} &= A_{os} \left[\frac{1 + R_{To}(R_s, R_l)/R_f}{1 + R_T(R_s, R_l)/R_f} \right] \\ &\approx -\left(\frac{g_{me} R - 1}{2} \right) \approx -\left[\frac{(R_f/R) - 1}{2} \right]. \end{aligned} \quad (9-120)$$

Observe that a gain magnitude exceeding unity requires $g_{me} R > 3$ or equivalently, $R_f > 3R$. Recalling Eq. (9-111), this constraint invariably mandates

that the transistor in the circuit diagram of Fig. 9.32(a) have sufficiently large gate aspect ratio and/or that it be biased at sufficiently large drain current.

It is also interesting to note that since the driving point input resistance, R_{in} , predicted by the model in Fig. 9.33(a) is R , provided that Eq. (9-119) and its companion approximations are satisfied, the ratio, V_i/V_s , of input port signal voltage to Thévenin signal source voltage is precisely $1/2$. Since the low frequency closed loop voltage gain, A_{vo} , can be written as $A_{vo} = V_{os}/V_s = (V_i/V_s)(V_{os}/V_i)$, Eq. (9-120) confirms a port voltage gain, say A_{io} , of

$$A_{io} = \frac{V_{os}}{V_i} \approx -(g_{me}R - 1). \quad (9-121)$$

The importance of this port gain is underscored in a subsequent subsection addressing the driving point input impedance of the subject amplifier.

9.7.2. Amplifier Bandwidth

If the feedback amplifier in Fig. 9.32(a) postures a dominant pole frequency response, its small signal voltage transfer function, $A_v(s)$, can be approximated at high signal frequencies by the single pole expression,

$$A_v(s) \approx \frac{A_{vo}}{1 + \frac{s}{B}}, \quad (9-122)$$

where, assuming match terminated design conditions, A_{vo} is the low frequency voltage gain stipulated by Eq. (9-120), and B , the approximate radial 3-dB bandwidth of the amplifier, is precisely the sum of the open circuit time constants associated with the three individual capacitances embedded in the model of Fig. 9.32(b). Specifically, parameter B derives from an expression of the form,

$$\frac{1}{B} = R_{gs}C_{gs} + R_{gd}C_{gd} + R_{cl}C_l. \quad (9-123)$$

With the signal source voltage, V_s , set to zero, R_{gs} is the resistance that effectively faces capacitance C_{gs} when $C_{gd} = C_l = 0$, R_{gd} is the effective resistance seen by C_{gd} when $C_{gs} = C_l = 0$, and finally, R_{cl} is the resistance effectively in shunt with capacitance C_l , under the condition of $C_{gs} = C_{gd} = 0$. Assuming that resistances R_i and R_o in the equivalent circuit are very large and that the feedback resistance, R_f , is chosen in

accordance with the match termination constraint in Eq. (9-119), the dividends of a bit of circuit analyses are

$$R_{gs} = \frac{1}{2} \left[\frac{R + R_{ss}}{1 + g_m R_{ss}} + \left(\frac{1}{1 + g_{me} R} \right) \left(\frac{R_{ss}}{1 + g_m R_{ss}} \right) \right], \quad (9-124)$$

$$R_{gd} = \left(\frac{2 + g_{me} R}{1 + g_{me} R} \right) \left(\frac{g_{me} R^2}{2} \right), \quad (9-125)$$

and

$$R_{cl} = \frac{R}{2}. \quad (9-126)$$

In the last expression, use is made of the fact that the load capacitance, C_l , shunts a terminating load resistance of R , as well as a low frequency driving point output resistance that is identical to R because of the design constraint imposed by Eq. (9-119). Assuming further that the design goal embraces a relatively large voltage gain magnitude at low frequencies, which mandates $g_{me} R \gg 1$, the combination of the preceding four expressions produces

$$B \approx \frac{2}{R(C_{gm} + C_{dm} + C_l) + R_{ss} C_{gm}}, \quad (9-127)$$

where

$$C_{gm} \triangleq \frac{C_{gs}}{1 + g_m R_{ss}} \quad (9-128)$$

and

$$C_{dm} \triangleq g_{me} R C_{gd}. \quad (9-129)$$

Observe that the effect of the transconductance feedback element, R_{ss} , is to reduce the effective value of transistor gate-source capacitance, C_{gs} . On the other hand, the transistor gate-drain capacitance, C_{gd} , is multiplied by the factor, $g_{me} R$, to which the transimpedance feedback element, R_f , is directly proportional and on which the low frequency voltage gain is linearly dependent. As is shown shortly, this factor is the Miller multiplier of capacitance C_{gd} ; that is, C_{dm} is approximately the value of input port capacitance when capacitance C_{gd} is referred to the input port. In most practical situations, $C_l \ll (C_{gm} + C_{dm})$. Accordingly, Eq. (9-127) reduces to

$$B \approx \frac{2}{R(C_{gm} + C_{dm}) + R_{ss} C_{gm}}. \quad (9-130)$$

9.7.3. Input Impedance

An expression for the driving point input impedance, Z_{in} , of the shunt-series feedback amplifier can be derived by applying the trustworthy mathematical ohmmeter method to the model shown in Fig. 9.32(b). Although this derivation is a straightforward exercise, it produces results whose algebraic complexity masks crucial design-oriented implications. A more insightful, but admittedly approximate, analytical strategy examines the loading imposed on the applied signal source by the two capacitances, C_{gs} and C_{gd} , in Fig. 9.32(b). To this end, the considered model is redrawn as Fig. 9.35(a) for the design objective of match terminated operation. The input port resistance, R_i , and its counterpart output port resistance, R_o , are presumed sufficiently large to justify their tacit neglect. Additionally, the small, match terminated open circuit time constant associated with the net load capacitance, C_l , encourages ignoring this capacitance.

In terms of the input and output port signal voltages, V_i and V_{os} , respectively, the current, I_{gd} , conducted by capacitance C_{gd} , which must be supplied by the Thévenin input voltage, is

$$I_{gd} = sC_{gd} (V_i - V_{os}) = sC_{gd} V_i \left(1 - \frac{V_{os}}{V_i} \right). \quad (9-131)$$

But since capacitance C_l is ignored, the ratio, V_{os}/V_i , is precisely the low frequency port gain given by Eq. (9-121), whence

$$\begin{aligned} I_{gd} &= sC_{gd} V_i \left(1 - \frac{V_{os}}{V_i} \right) = sC_{gd} V_i (1 - A_{io}) \\ &= s g_{me} R C_{gd} V_i = s C_{dm} V, \end{aligned} \quad (9-132)$$

where Eq. (9-129) is recalled. Thus, the signal current supplied to C_{gd} by the signal voltage, V_s , is equivalent to the current conducted by an effective capacitance, C_{dm} , which is incident between the input port and ground. The alternative model depicted in Fig. 9.35(b) reflects this observation.

An analytical strategy similar to that just executed with respect to C_{gd} can be applied to capacitance C_{gs} in the model of Fig. 9.35(a). In particular, the input port voltage, V_i , is

$$V_i = V_1 + R_{ss} (g_m V_1 + s C_{gs} V_1),$$

which portends

$$V_1 = \frac{V_i}{1 + g_m R_{ss} + s R_{ss} C_{gs}}. \quad (9-133)$$

be noted that Eq. (9-133) allows the controlled current, $g_m V_1$, to be rendered proportional to the input port voltage, V_i , in accordance with

$$g_m V_1 = \frac{g_m V_i}{1 + g_m R_{ss} + s R_{ss} C_{gs}} = \frac{g_{me} V_i}{1 + s R_{ss} C_{gm}}, \tag{9-135}$$

where Eqs. (9-111) and (9-128) have been invoked. The electrical implications of Eqs. (9-134) and (9-135) are mirrored topologically by the alternative high frequency model in Fig. 9.35(b).

The model just derived clearly suggests that the input impedance, Z_{in} , of the shunt-series feedback amplifier is capacitive. An approximate expression for this impedance function can be straightforwardly deduced if the radial signal frequencies, ω , of interest are constrained to satisfy the inequality, $\omega R_{ss} C_{gm} \ll 1$. Under this circumstance, the impedance indicated as Z_i in Fig. 9.35(b) reduces to the low frequency value of Z_{in} , which has already been shown to be R for the match terminated case under investigation. Accordingly, Z_{in} is little more than the impedance of the parallel combination of R , capacitance C_{dm} , and the series interconnection of resistance R_{ss} and capacitance C_{gm} ; that is,

$$Z_{in} \approx \frac{R (1 + s R_{ss} C_{gm})}{1 + s [R_{ss} C_{gm} + R (C_{gm} + C_{dm})] + s^2 R R_{ss} C_{gm} C_{dm}}. \tag{9-136}$$

Note that for small R_{ss} , this result implies an effective input port capacitance, C_{in} , of

$$C_{in} \approx C_{gm} + C_{dm} = \frac{C_{gs}}{1 + g_m R_{ss}} + g_{me} R C_{gd}. \tag{9-137}$$

9.7.4. Input Impedance Compensation

The input impedance degradation with frequency of the match terminated shunt-series feedback amplifier confirms the logical suspicion that impedance matching prevails at only low signal frequencies. At higher frequencies, the effect of a reduced input impedance magnitude is an amplifier input port voltage that is progressively smaller for a given Thévenin source voltage and is therefore in danger of falling below the detectable level determined by the equivalent input noise voltage, or *noise floor*, of the amplifier.^[9] The remedy is a matching filter interposed, as suggested by Fig. 9.36(a), between the signal source and the input port of the amplifier. In an ideal world, this filter minimally satisfies two operational constraints. First, the driving point impedance, Z_a , seen looking into its input terminals is constant at a value equal to the match terminated Thévenin source

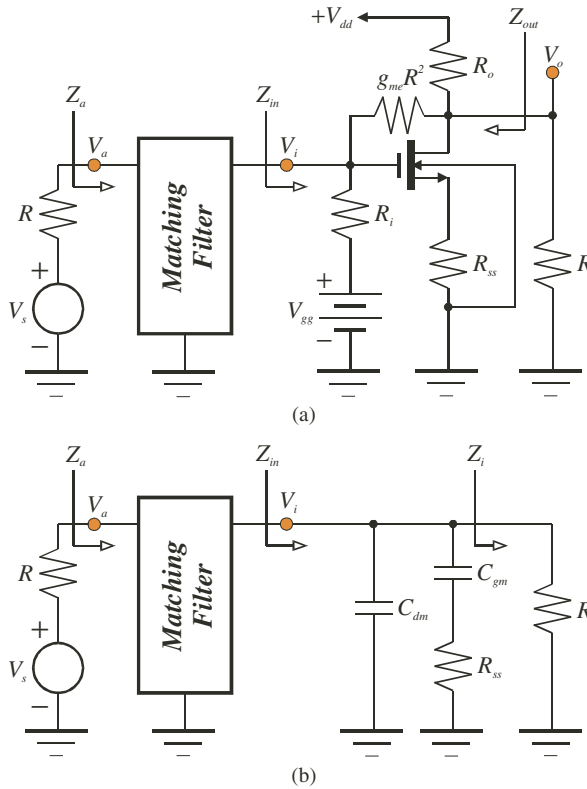


Figure 9.36. (a) The shunt-series feedback amplifier of Fig. 9.32(a), which incorporates an input port matching filter to compensate for the frequency dependence of the input impedance, Z_{in} . (b) The approximate input port model of the amplifier, wherein the results underlying the topology of Fig. 9.35(b) have been exploited.

resistance, R , for all signal frequencies of interest. Second, the filter should deliver a port voltage transfer function, V_i/V_a , of unity, or at least close to one, so that minimal loss of gain is incurred between the applied signal excitation and the amplifier input terminals. If both these performance objectives are met, maximum signal power transfer is assured between the signal source and the filter input port, which supports a signal level nominally mirroring that observed at the amplifier input port; that is, $V_i \approx V_a$. Using the results deduced in the preceding subsection, a viable input port model is the structure appearing in Fig. 9.36(b). The latter model is approximate in that $Z_i \approx R$ only if $\omega R_{ss} C_{gm} \ll 1$.

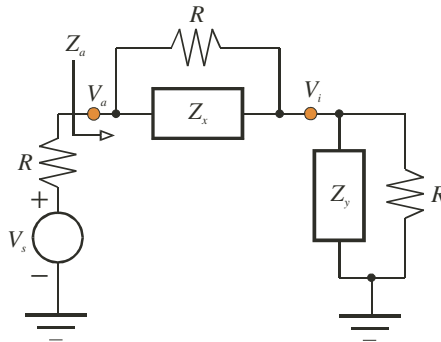


Figure 9.37. A plausible matching filter for the input port of the shunt-series amplifier of Fig. 9.36(a).

The technical literature is sprinkled with a number of filters that satisfy the foregoing proscribed requirements.^[10] For the application at hand, a leading filter candidate is the architecture shown in Fig. 9.37, for which the indicated input impedance, Z_a , is identical to the resistance, R , provided that impedances Z_x and Z_y are the scaled duos implied by the constraint,

$$Z_x Z_y = R^2. \tag{9-138}$$

It is a simple matter to show that Eq. (9-138) stipulates a filter voltage transfer function, V_i/V_a , of

$$\frac{V_i}{V_a} = \frac{1}{1 + \frac{R}{Z_y}} \equiv \frac{1}{1 + \frac{Z_x}{R}}. \tag{9-139}$$

When adapted to the input port model of Fig. 9.36(b), the compensated configuration becomes the network offered in Fig. 9.38(a). The interesting feature of this adaptation is that impedance Z_y is not a designable element and is, in fact, the impedance associated with the parallel interconnection of capacitance C_{dm} and the series combination of resistance R_{ss} and capacitance C_{gm} . Specifically,

$$Z_y = \frac{\left(\frac{1}{sC_{dm}}\right) \left(R_{ss} + \frac{1}{sC_{gm}}\right)}{\frac{1}{sC_{dm}} + R_{ss} + \frac{1}{sC_{gm}}} = \frac{1 + sR_{ss}C_{gm}}{s(C_{gm} + C_{dm}) + s^2R_{ss}C_{gm}C_{dm}}. \tag{9-140}$$

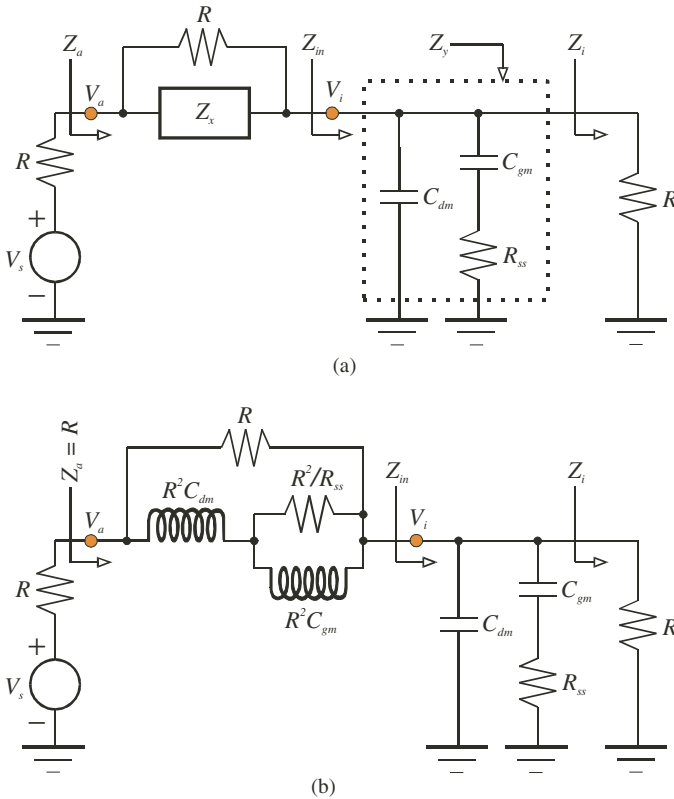


Figure 9.38. (a) The matching filter of Fig. 9.37 adapted for the input port of the shunt-series feedback amplifier. (b) The realization of impedance Z_x in the filter of (a).

It follows from Eq. (9-138) that the impedance, Z_x , required for matched compensation is

$$\begin{aligned}
 Z_x &= \frac{R^2 [s(C_{gm} + C_{dm}) + s^2 R_{ss} C_{gm} C_{dm}]}{1 + s R_{ss} C_{gm}} \\
 &= s R^2 C_{dm} + \frac{1}{\frac{R_{ss}}{R^2} + \frac{1}{s R^2 C_{gm}}}, \tag{9-141}
 \end{aligned}$$

which suggests the realization delineated in Fig. 9.38(b). Figure 9.39 shows the basic schematic diagram of the shunt-series feedback amplifier that results when the input port matching filter is incorporated. Also incorporated into the compensated structure is a suitably large blocking capacitor,

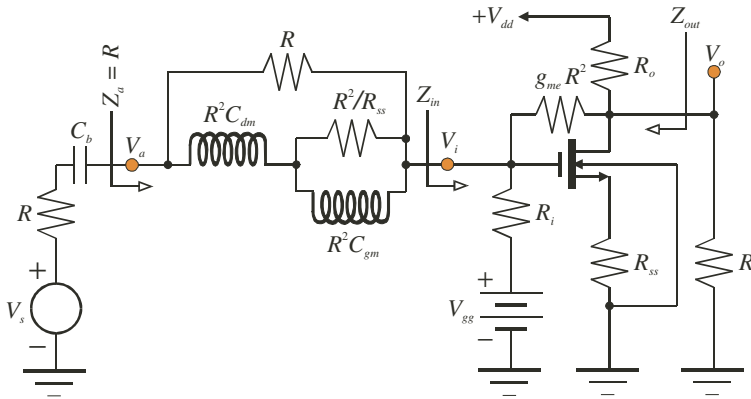


Figure 9.39. The shunt-series feedback amplifier of Fig. 9.32(a) with an input matching filter incorporated to compensate for the frequency dependence of the indicated amplifier input port impedance, Z_{in} .

C_b , to prevent static current flow through the applied signal source. Observe that the inductance, $R^2 C_{dm}$, can be implemented as a bond wire of suitable length and cross section area.

It should be noted in Fig. 9.38(a) that the input impedance, Z_{in} , seen looking into the gate of the transistor in the shunt-series feedback amplifier is little more than the parallel combination of the impedance, Z_y , and the resistance R , which is to say that

$$Z_y = \frac{R Z_{in}}{R - Z_{in}}. \tag{9-142}$$

If this relationship is substituted into Eq. (9-139), the voltage transfer function from the filter input port to the amplifier input port is simply

$$\frac{V_i}{V_a} = \frac{Z_{in}}{R}. \tag{9-143}$$

Since the impedance indicated as Z_a in Fig. 9.38(b) is R , $V_a/V_s = 1/2$, independent of signal frequency. With the load capacitance, C_l , tacitly ignored and with the forward characteristics of the amplifier at hand modeled by the approximate equivalent circuit shown in Fig. 9.35(b), the port gain, V_{os}/V_i , of the amplifier is given by Eq. (9-121), assuming that $\omega R_{ss} C_{gm} \ll 1$.

It follows that the overall I/O gain of the amplifier is

$$A_v(s) = \frac{V_{os}}{V_s} = \frac{V_{os}}{V_i} \times \frac{V_i}{V_a} \times \frac{V_a}{V_s} \approx - \left(\frac{g_{me}R - 1}{2} \right) \times \left\{ \frac{1 + sR_{ss}C_{gm}}{1 + s[R_{ss}C_{gm} + R(C_{gm} + C_{dm})] + s^2RR_{ss}C_{gm}C_{dm}} \right\}. \quad (9-144)$$

Equation (9-144) confirms that the incorporation of the matching filter at the amplifier input port does not degrade the zero frequency closed loop gain, A_{vo} , stipulated earlier as Eq. (9-120). It also confirms that because of the left half plane zero, the magnitude response rolls off with high signal frequencies at a rate of only 20 dB/decade, despite the inherently second order nature of the circuit used to model the active network. Recall that this frequency characteristic is desirable from the perspective of ensuring adequate gain and phase margins in the closed loop response. Unfortunately, however, Eq. (9-144) underscores a drawback to the use of the input port filter. In particular, Eqs. (9-120) and (9-130) allow Eq. (9-144) to be written in the form,

$$A_v(s) \approx \frac{A_{vo}(1 + sR_{ss}C_{gm})}{1 + \frac{2s}{B} + s^2RR_{ss}C_{gm}C_{dm}}, \quad (9-145)$$

whose first order term in the indicated characteristic polynomial suggests, assuming that time constant $R_{ss}C_{gm}$ is small, an approximate radial bandwidth of $B/2$. Accordingly, a deleterious impact of the utilized matching filter is that the approximate bandwidth, B , achieved without the matching filter, is reduced by a factor of two.

Example 9.6. The shunt-series feedback amplifier depicted in Fig. 9.32 is to be designed to deliver a low frequency voltage gain magnitude of five (14 dB) when operated match terminated into 50 ohms. The transistor used has a short circuit unity gain frequency (f_T) of 35 GHz, a drain-source channel resistance (r_o) of 25 K Ω , and a bulk-induced threshold modulation factor (λ_b) of 0.025. For the given semiconductor process, the gate-drain capacitance is known to be roughly 15% of the gate-source capacitance. An estimate of the parasitic load capacitance (C_l) (inclusive of bulk-drain device capacitance) is 300 fF. Design the basic cell by calculating an appropriate value of the transconductance feedback resistance, R_{ss} , the required value of the transresistance feedback element, R_f , and the values of gate-source and gate-drain capacitances, C_{gs} and C_{gd} , respectively, appropriate to the geometry and biasing levels that produce the device transconductance,

g_m , required of the amplifier. Additionally, estimate the 3-dB bandwidth of the amplifier, divorced of any matching filter implemented at the input signal port. Submit two designs: one without an input impedance matching filter and one with an appropriate input filter embedded. Compare the small signal performance of the two designs through HSPICE simulations.

Solution 9.6.

- (1) With a gain magnitude, $|A_{vo}|$, of 5 and for $R = 50 \Omega$, Eq. (9-120) gives a required effective transconductance of $g_{me} = 220$ mmhos. Because of Eq. (9-111), the source lead resistance, R_{ss} , must be smaller than $1/g_{me}$, which is 4.545Ω in this case. Select $R_{ss} = 2.5 \Omega$, which requires, again by Eq. (9-111),

$$g_m = \frac{g_{me}}{1 - g_{me} R_{ss}} = 488.9 \text{ mmhos.} \quad (\text{E6-1})$$

Since the analyses undertaken as a prelude to this example ignore drain-source channel resistance, bulk-induced threshold voltage modulation, and several other second order factors, it is prudent to increase the computed device transconductance value by 5% or so. In view of this strategy, let $g_m = 510$ mmhos.

- (2) From Eq. (9-119) and using $g_m = 510$ mmhos, the requisite voltage feedback resistance is $R_f = 560.4 \Omega$.
- (3) Recall that for the purpose of this demonstration, $C_{gd} = 0.15 C_{gs}$. Then, the unity gain radial frequency, $\omega_T = 2\pi f_T$, is stipulated by

$$\omega_T = \frac{g_m}{C_{gs} + C_{gd}} = \frac{g_m}{1.15 C_{gs}}. \quad (\text{E6-2})$$

Given $g_m = 510$ mmhos and $\omega_T = 2\pi(35 \text{ GHz})$, C_{gs} must be $C_{gs} = 2.017 \text{ pF}$, which means that $C_{gd} = 0.15 C_{gs} = 302.5 \text{ fF}$.

- (4) Using Eqs. (9-128) and (9-129), $C_{gm} = 886.4 \text{ fF}$ and $C_{dm} = 3.391 \text{ pF}$.
- (5) With respect to the elements of the input matching filter drawn in Fig. 9.39, $R^2 C_{dm} = 8.319 \text{ nH}$, $R^2 C_{gm} = 2.216 \text{ nH}$, and $R^2/R_{ss} = 1 \text{ K}\Omega$.
- (6) From Eq. (9-127), the estimated 3-dB bandwidth of the amplifier operated without the input port filter is $B = 2\pi(1.378 \text{ GHz})$.
- (7) The foregoing design calculations precipitate Fig. 9.40, which shows the resultant small signal model schematic of the shunt-series amplifier. In order to facilitate future analyses and assessments, the output impedance, Z_{out} , is here-with redefined as the impedance effectively facing the shunt interconnection of the terminating load resistance, R , and the net load capacitance, C_l . With switch SW closed in this diagram, the amplifier operates without benefit of broadband input impedance matching. On the other hand, SW open activates the input port matching filter.

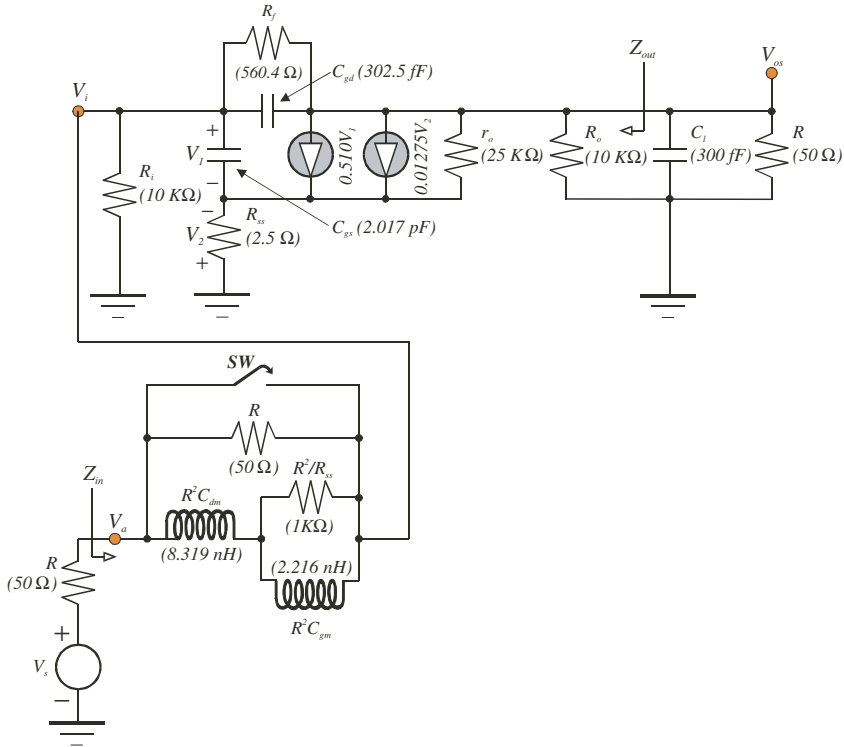


Figure 9.40. The schematic diagram of the small signal model of the shunt-series feedback amplifier designed in Example 9.6. With switch SW open, the amplifier operates with an input port impedance matching filter incorporated. A closed switch constrains the amplifier to operate without an input port filter.

Comments. Figure 9.41 displays the pertinent magnitude responses for the cases of input impedance matching and no matching filter implemented. Both responses show a low frequency gain of 14.04 dB, or 5.04 volts/volt, which is higher than the design goal of 5.0 volts/volt by only 0.80%. Obviously, the tack of increasing the originally computed device transconductance by 5% has proven minutely over zealous. For the case of no input port impedance matching, the simulated 3-dB bandwidth is 1.374 GHz, a scant 4 MHz lower than the design estimate of 1.378 GHz. This miniscule computational error confirms that the considered amplifier behaves as a dominant pole structure, despite its inherent third order nature and the presence of a finite frequency left half plane zero. With input port matching, the simulated bandwidth is 717.6 MHz, which is smaller than the non-matched simulated bandwidth by a factor of 1.92. In theory, the subject bandwidth ratio should be two. This slight disparity between simulated and computed bandwidth ratio can doubtlessly be attributed to the “Miller time” method invoked with respect to

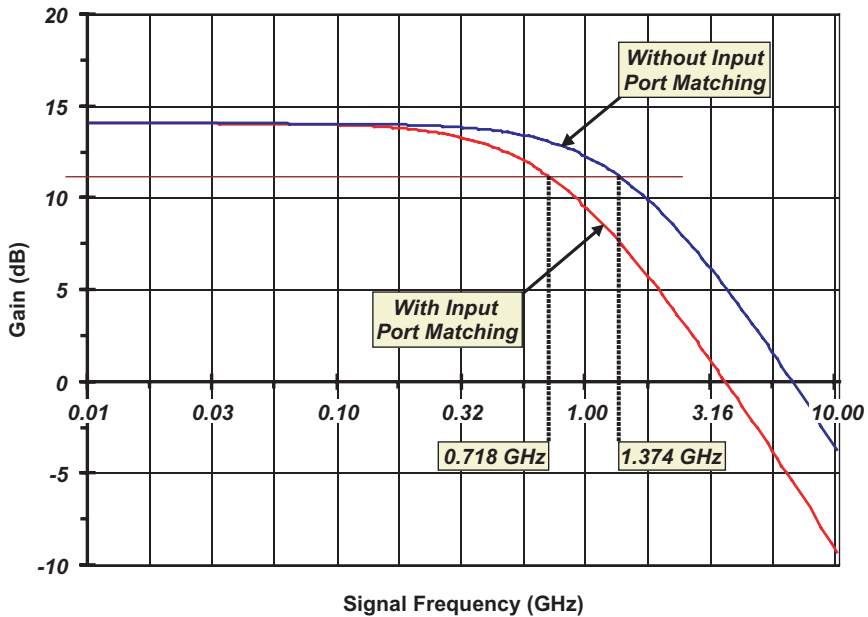


Figure 9.41. The frequency responses of the shunt-series feedback amplifier whose small signal equivalent circuit is diagrammed in Fig. 9.40. The curve labeled, “without input port matching,” corresponds to switch *SW* closed in Fig. 9.40. The curve indicated “with input port matching” pertains to the case of switch *SW* open circuited in the aforementioned modeling diagram.

representing the transistor gate-drain capacitance as an effective input port capacitance. Also, recall that several approximations (neglect of channel resistance, neglect of bulk-induced threshold voltage modulation, etc.) were exploited in the course of all theoretic analyses.

The magnitude of the driving point input impedances, both with and without input port matching, are exhibited in Fig. 9.42. In both cases, the simulated low frequency values of the input impedance are 50.63Ω , which differs from the design objective by only 1.26%. Without impedance matching, the input impedance magnitude plummets to roughly 25Ω at the 3-dB bandwidth of the amplifier. A detailed analysis of the simulated data for the nonmatched case reveals a capacitive input impedance over all frequencies of interest. This capacitance characteristic is depicted in Fig. 9.43. Observe a low frequency input capacitance of about 3.68 pF, which is slightly larger than capacitance C_{dm} , but smaller than the capacitance sum, $(C_{dm} + C_{gm})$. This observation synergizes with the input port model postulated in Fig. 9.38. With input port matching, the input impedance magnitude remains at its low frequency value to within about 5Ω through the entire range of considered

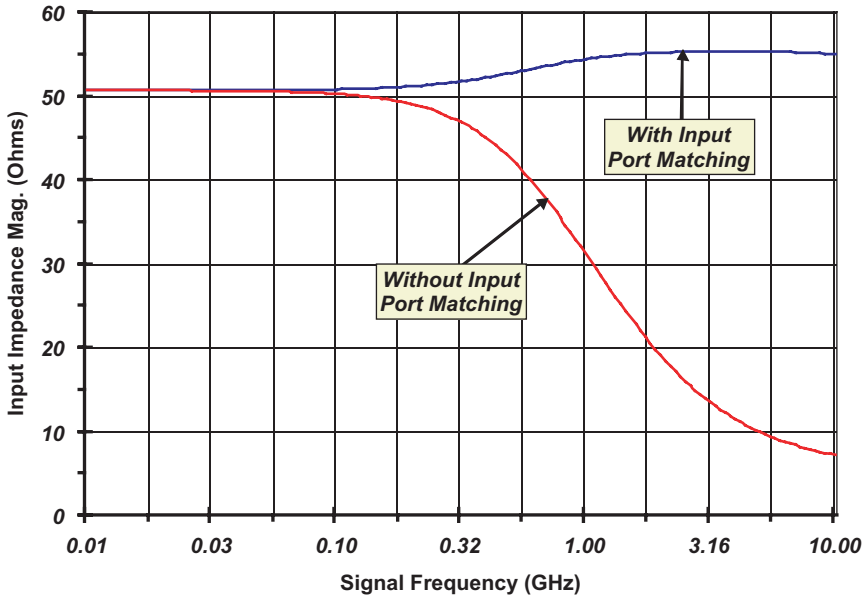


Figure 9.42. The magnitude of the input impedance for the shunt-series feedback amplifier modeled in Fig. 9.40. The curve labeled, “without input port matching,” corresponds to switch SW closed in the subject model. The curve indicated “with input port matching” pertains to the case of switch SW open circuited.

signal frequencies. In contrast to the nonmatched circumstance, the matched input impedance is slightly inductive through, and substantially beyond, the amplifier 3-dB bandwidth. In view of the clearly inductive impedance that appears in series with the input port in Fig. 9.38, this state of affairs is hardly surprising.

9.7.5. Output Impedance

The output impedance, Z_{out} , seen by the terminating load resistance, R , and the net load capacitance, C_l , in the shunt-series feedback amplifier under consideration is simply the ratio, V_x/I_x , in the model of Fig. 9.44(a). If this impedance, whose low frequency value has already been established to be the matching resistance, R , is approximated as a first order frequency function,

$$Z_{out} \approx R \left(\frac{1 + as}{1 + bs} \right), \tag{9-146}$$

where parameter “a” is the sum of the open circuit time constants associated with the impedance zeros, while parameter “b” is the sum of the open circuit

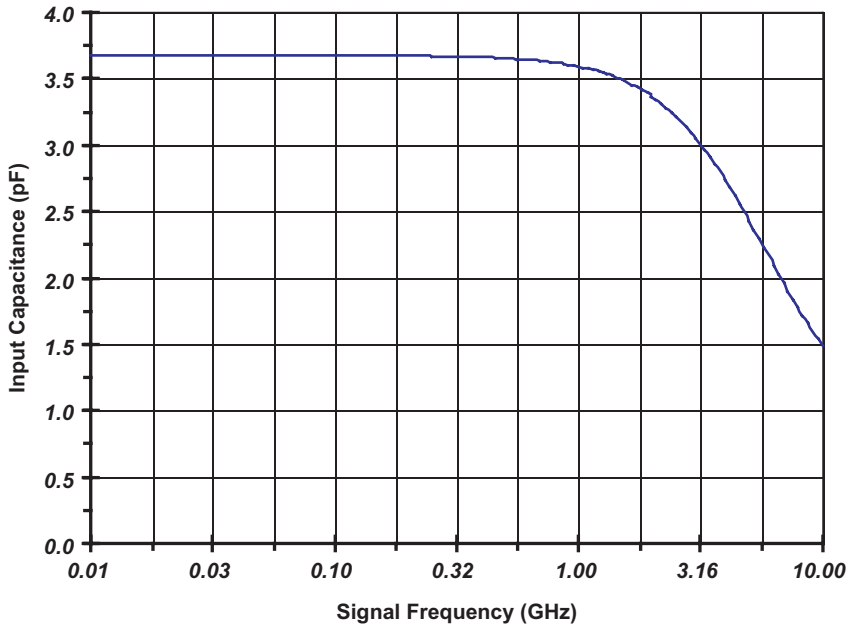


Figure 9.43. The input port capacitance of the shunt series modeled by the circuit structure in Fig. 9.40. For this capacitance simulation, switch SW in the aforementioned diagram remains closed; that is, no input port matching filter is utilized.

time constants associated with the poles of the output impedance.^[11] With reference to the equivalent circuit in Fig. 9.44(b), parameters “a” and “b” are given precisely by

$$\left. \begin{aligned}
 a &= C_{gs} \left(\frac{V_1}{I_1} \Big|_{V_x=0} \right) + C_{gd} \left(\frac{V_2}{I_2} \Big|_{V_x=0} \right) \\
 b &= C_{gs} \left(\frac{V_1}{I_1} \Big|_{I_x=0} \right) + C_{gd} \left(\frac{V_2}{I_2} \Big|_{I_x=0} \right)
 \end{aligned} \right\}, \tag{9-147}$$

where each of the parenthesized voltage to current ratios is recognized as an effective resistance facing the corresponding multiplicative capacitance under the condition of either a short circuited ($V_x = 0$) or an open circuited ($I_x = 0$) output port. Assuming large R_i and R_o , the execution of analyses commanded by Eq. (9-147) results in

$$a = \left(\frac{g_{me} R^2}{1 + g_{me} R} \right) C_{gm} + \left(\frac{R}{1 + g_{me} R} \right) C_{dm} \tag{9-148}$$

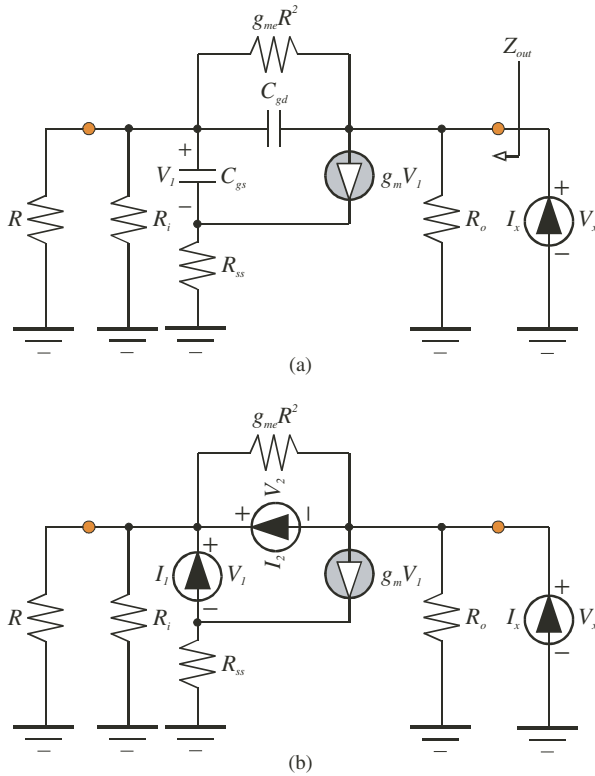


Figure 9.44. (a) Model used to evaluate the driving point output impedance, Z_{out} , of the shunt-series feedback amplifier. (b) Model exploited to calculate the time constants of the pole and zero associated with a first order frequency domain representation of the output impedance.

and

$$b = \left(\frac{R + R_{ss}}{1 + g_{me}R} \right) C_{gm} + RC_{dm}, \tag{9-149}$$

where the effective transconductance and capacitance values, g_{me} , C_{gm} , and C_{dm} , are given respectively by Eqs. (9-111), (9-128), and (9-129).

A tacit inspection of Eq. (9-146) reveals that the driving point output impedance is inductive for $a > b$, purely resistive for $a = b$, and capacitive for $a < b$. From Eqs. (9-148) and (9-149), the inductive condition of $a > b$ requires

$$\frac{C_{gm} - C_{dm}}{C_{gm}} = \frac{C_{gs} - g_{me}R(1 + g_m R_{ss})C_{gd}}{C_{gs}} > \frac{R + R_{ss}}{g_{me}R^2}, \tag{9-150}$$

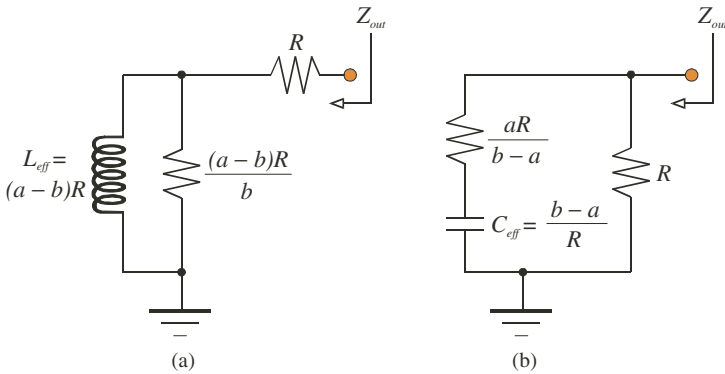


Figure 9.45. (a) Passive representation of an inductive driving point output impedance for the shunt-series feedback amplifier. (b) Passive representation of a capacitive driving point output impedance for the shunt-series feedback amplifier.

for which a necessary condition of satisfaction is

$$\frac{C_{gs}}{C_{gd}} > g_{me} R(1 + g_m R_{ss}). \tag{9-151}$$

Note that an inductive output impedance in the shunt-series feedback amplifier is likely to derive from the sufficiently small gate-drain capacitance, C_{gd} , achieved with self-aligned gate processing. Obviously, a capacitive output impedance follows from the dissatisfaction of Eq. (9-150).

For the inductive case of $a > b$, a meaningful expansion of Eq. (9-146) is

$$Z_{out} \approx R \left(\frac{1 + as}{1 + bs} \right) = R + \frac{1}{\frac{1}{R} \left(\frac{b}{a-b} \right) + \frac{1}{R(a-b)s}}, \tag{9-152}$$

whose passive realization is given in Fig. 9.45(a). Observe an effective inductance, L_{eff} , of

$$L_{eff} = R(a-b) = \left(\frac{g_{me} R}{1 + g_{me} R} \right) R^2 \times \left[(C_{gm} - C_{dm}) - \left(1 + \frac{R_{ss}}{R} \right) \left(\frac{C_{gm}}{g_{me} R} \right) \right]. \tag{9-153}$$

For large $g_{me} R$, which is tantamount to stipulating a relatively large voltage gain at low signal frequencies,

$$L_{eff} \approx R^2(C_{gm} - C_{dm}). \tag{9-154}$$

In the capacitive case of $a < b$, a continued fraction expansion of Eq. (9-146) is

$$Z_{out} \approx R \left(\frac{1 + as}{1 + bs} \right) = \frac{1}{\frac{1}{R} + \frac{1}{\frac{aR}{b-a} + \frac{1}{(b-a)s}}}, \quad (9-155)$$

whose passive representation appears in Fig. 9.45(b). The effective capacitance, C_{eff} , associated with this passive model is

$$C_{eff} = \frac{b-a}{R} = \left(\frac{g_{me}R}{1 + g_{me}R} \right) \times \left[(C_{dm} - C_{gm}) + \left(1 + \frac{R_{ss}}{R} \right) \left(\frac{C_{gm}}{g_{me}R} \right) \right]. \quad (9-156)$$

For the large gain circumstance implied by large $g_{me}R$,

$$C_{eff} \approx C_{dm} - C_{gm}. \quad (9-157)$$

Example 9.7. In the shunt-series feedback amplifier depicted in Fig. 9.32 and analyzed in Example 9.6, examine the resultant driving point output impedance. In particular, determine whether this output impedance is inductive or capacitive for the case of no broadband impedance matching implemented at the amplifier input port. Using the small signal model shown in Fig. 9.40, simulate the output impedance with HSPICE, and compare these simulated results with simulations executed on the appropriate macromodel offered in Fig. 9.45. For ease of reference, the pertinent results gleaned in the preceding example are listed herewith.

$g_m = 510 \text{ mmhos}$	$g_{me} = 224.18 \text{ mmhos}$
$C_{gs} = 2.017 \text{ pF}$	$C_{gd} = 302.5 \text{ fF}$
$C_{gm} = 886.4 \text{ fF}$	$C_{dm} = 3.391 \text{ pF}$
$R_f = 560.4 \text{ ohms}$	$R_{ss} = 2.5 \text{ ohms}$
$\lambda_b = 0.025$	$r_o = 25 \text{ Kohms}$
$R_i = 10 \text{ Kohms}$	$R_o = 10 \text{ Kohms}$

Solution 9.7.

- (1) An assessment of the nature of the driving point output impedance requires only that parameters “ a ” and “ b ” in Eqs. (9-148) and (9-149) be compared. To this end, $a = 54.577 \text{ pSEC}$ and $b = 173.34 \text{ pSEC}$. Since $a < b$, the output impedance is capacitive.

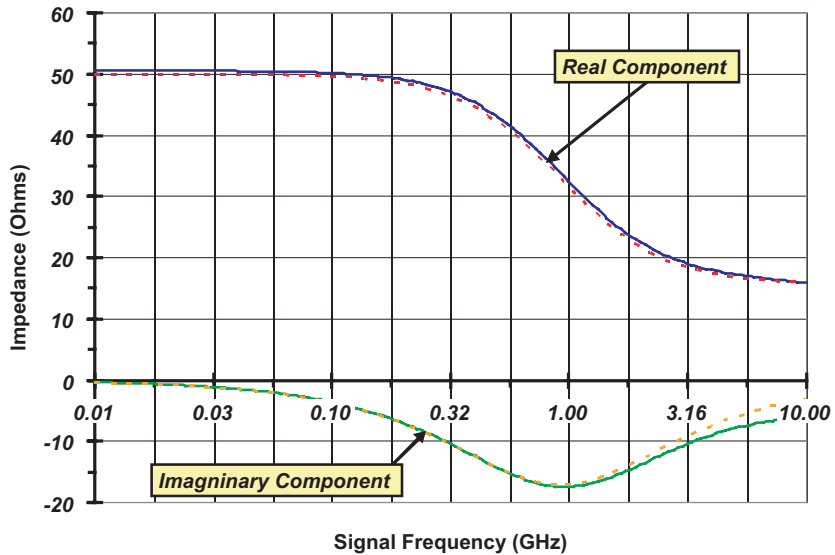


Figure 9.46. The simulated real part and imaginary part components of the driving point output impedance of the shunt-series feedback amplifier addressed in Examples 9.6 and 9.7. The solid curves correspond to the physically sound, small signal model of the amplifier shown in Fig. 9.40. The dashed curves reflect simulations executed on the impedance macromodel of Fig. 9.45(b).

(2) Since the output impedance is capacitive, the pertinent output port representation is the schematic diagram of Fig. 9.45(b). In this diagram,

$$\left. \begin{aligned}
 R &= 50 \Omega \\
 \frac{aR}{b-a} &= 22.977 \Omega \\
 C_{eff} &= \frac{b-a}{R} = 2.375 \text{ pF}
 \end{aligned} \right\} .$$

(3) The HSPICE simulations of the real and imaginary parts of the output impedance are shown in Fig. 9.46 for both the amplifier model of Fig. 9.40 and the impedance macromodel of Fig. 9.45(b).

Comments. The simulated results shown in Fig. 9.46 confirm the capacitive nature of the driving point output impedance for the shunt-series feedback amplifier in that the imaginary component of the subject impedance is negative for all signal frequencies of interest. The excellent agreement between the simulated results gleaned from the actual small signal equivalent circuit and the impedance macromodel is cause for celebration. Specifically, this agreement verifies the propriety of

the dominant pole/dominant zero strategy adopted to assess the output impedance characteristics over frequency.

9.8.0. The f_T -Doubler

In most open loop amplifiers, such as the series peaked and series-shunt peaked configurations studied earlier, the achievable 3-dB bandwidth is limited by the effective load capacitance incident at the amplifier output port. On the other hand, the bandwidth of many closed loop amplifiers, for which a notable example is the dual loop feedback network examined in the preceding section, is invariably determined by the intrinsic capacitances of the utilized transistors. In these latter topologies, an f_T -doubler, which is essentially a Darlington configuration designed to deliver nominally twice the unity gain frequency afforded by the single transistor it replaces, can be gainfully exploited for broadbanding purposes. The principle underlying the operation of these doublers is elementary. In particular, the short circuit, unity gain frequency, ω_T , of a MOSFET characterized by a forward transconductance of g_m , a net gate-source capacitance of C_{gs} , and a net gate-drain capacitance of C_{gd} is

$$\omega_T = 2\pi f_T = \frac{g_m}{C_{gs} + C_{gd}}. \quad (9-158)$$

If a circuit is contrived to double f_T while maintaining constant g_m , which is determined by geometry and biasing considerations, capacitances C_{gs} and C_{gd} are necessarily halved. To the extent that circuit bandwidth is linearly related to the gate-source and gate-drain capacitances of the transistor supplanted by the f_T -doubler, the observable 3-dB bandwidth is consequently doubled.

Figure 9.47 shows the basic schematic diagram of the f_T -doubler. A clue as to the alleged effectiveness of the circuit derives from observing that the small signal, high frequency impedance seen looking into the gate terminal of transistor $M1$ is rendered much larger than the gate to source impedance of $M1$ alone by the small signal series interconnection of the $M1$ source terminal with the $M2$ gate terminal. Since the high frequency gate-source impedance is dictated by gate-source capacitance and Miller-multiplied gate-drain capacitance, the effective values of these device capacitances are necessarily reduced by the aforementioned series topology. Maximal effectiveness of the circuit requires that transistors $M1$ and $M2$ be identical active devices having identical gate aspect ratios. When these transistors are biased in their saturation regimes at the same current, I_K , their indicated interconnection behaves as an effective single MOSFET, Me , whose unity gain

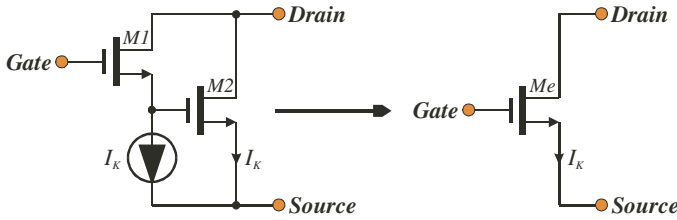


Figure 9.47. Basic schematic diagram of an f_T -doubler. Transistors $M1$ and $M2$ are identical devices biased in saturation at identical currents. The substrate terminals of both transistors are connected to the most negative potential afforded by the circuit in which the doubler is immersed. The doubler on the left behaves as an effective transistor, Me , whose unity gain frequency is nominally twice as large as the unity gain frequency of either transistors $M1$ or $M2$.

frequency, ω_e , is roughly twice ω_T , the unity gain frequency of $M1$ and $M2$, individually. In actual practice, ω_e is slightly less than $2\omega_T$, but approaches ω_T if the gate-drain capacitance of $M1$ (or of $M2$) is significantly smaller than the gate-source capacitance, C_{gs} , of each of these two devices.

9.8.1. Small Signal Analysis

A determination of the effective unity gain frequency, ω_e , of the structure given in Fig. 9.47 demands that its short circuit current gain, $A_{sc}(s) = I_{sc}/I_s$, be investigated as a function of signal frequency. To this end, the pertinent schematic diagram, divorced of biasing complexities, is provided in Fig. 9.48(a), for which the corresponding small signal model is the network in Fig. 9.48(b). The model in question takes the liberties of ignoring channel length modulation, bulk-induced threshold voltage modulation, transistor bulk-drain capacitances, and transistor bulk-source capacitances.

A straightforward analysis of the model in Fig. 9.48(b) results in the somewhat formidable transfer function,

$$\begin{aligned}
 A_{sc}(s) &= \frac{I_{sc}}{I_s} \\
 &= \left(\frac{\omega_T}{s}\right)^2 \left\{ \frac{1 + \frac{s}{\omega_T} \left(\frac{2C_{gs} - C_{gd}}{C_{gs} + C_{gd}}\right) - \left(\frac{s}{\omega_T}\right)^2 \left[\frac{C_{gd}(3C_{gs} + C_{gd})}{(C_{gs} + C_{gd})^2}\right]}{1 + \frac{C_{gd}C_{gs}}{(C_{gs} + C_{gd})^2} + \left(\frac{\omega_T}{s}\right) \left(\frac{C_{gd}}{C_{gs} + C_{gd}}\right)} \right\},
 \end{aligned}
 \tag{9-159}$$

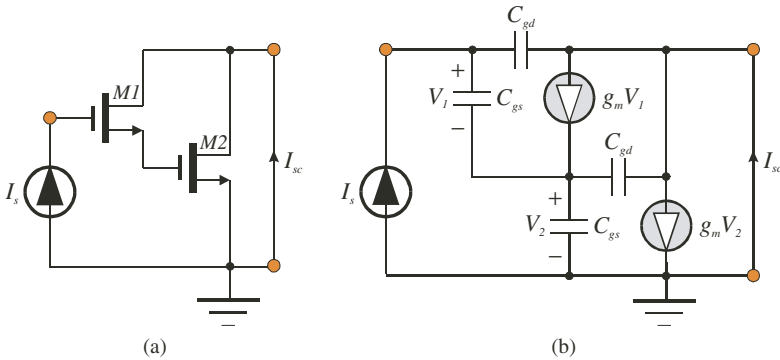


Figure 9.48. (a) The f_T -doubler circuit of Fig. 9.47 configured for an evaluation of the small signal, short circuit current gain, I_{sc}/I_s . (b) The approximate equivalent circuit for the network in (a).

where ω_T is given by Eq. (9-158) and is understood to be the unity gain frequency of either transistor $M1$ or $M2$ in the schematic diagram of Fig. 9.47. Assuming $C_{gd} \ll C_{gs}$ and given that interest herewith focuses on frequencies beyond ω_T , Eq. (9-159) can be approximated as

$$A_{sc}(s) \approx \left(\frac{\omega_T}{s}\right)^2 + \frac{2\omega_T}{s}, \tag{9-160}$$

which for sinusoidal excitation in the steady state becomes

$$A_{sc}(j\omega) \approx -\left(\frac{\omega_T}{\omega}\right)^2 - j2\left(\frac{\omega_T}{\omega}\right). \tag{9-161}$$

The resultant unity gain frequency, ω_e , is such that

$$|A_{sc}(j\omega_e)| = \sqrt{\left(\frac{\omega_T}{\omega_e}\right)^4 + 4\left(\frac{\omega_T}{\omega_e}\right)^2} \equiv 1, \tag{9-162}$$

for which the pertinent solution is

$$\frac{\omega_e}{\omega_T} = 2.058; \tag{9-163}$$

that is, the unity gain frequency of the doubler circuit is nominally twice that of the individual transistors embedded in the doubler. The exact solution for the doubler unity gain frequency, derived from a steady state sinusoidal analysis of Eq. (9-159), reveals that the frequency ratio, ω_e/ω_T , is a non-monotonic, but not especially sensitive, function of the capacitance ratio,

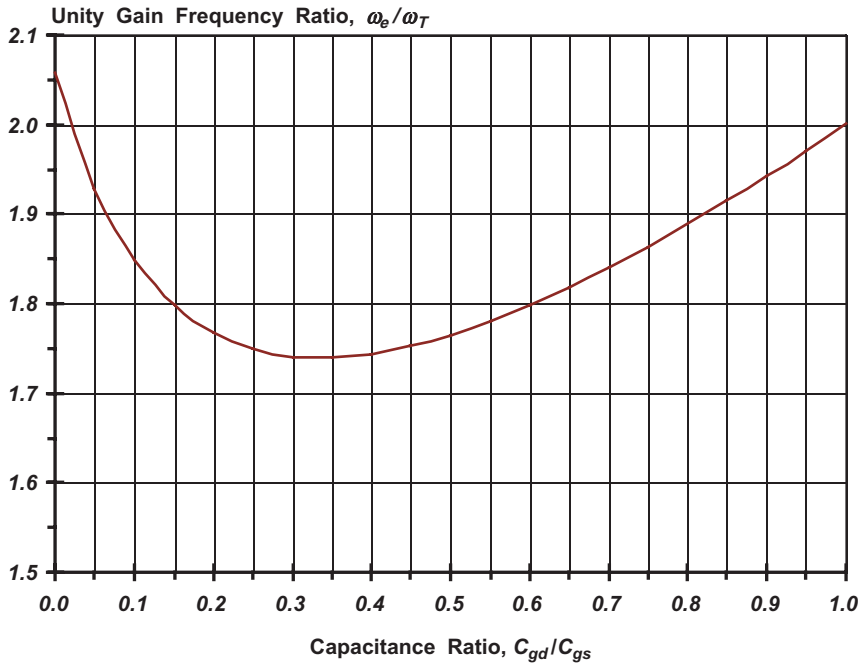


Figure 9.49. The unity gain frequency of the f_T -doubler in Fig. 9.47, normalized to the unity gain frequency of transistor $M1$ (or $M2$), viewed as a function of the gate-drain to gate-source capacitance ratio, C_{gd}/C_{gs} . The results reflect computer-aided analyses of the short circuit current transfer function of a doubler circuit that utilizes transistors deriving from a 28 GHz monolithic process.

C_{gd}/C_{gs} . Figure 9.49 is a graphical depiction of this functional dependence for the case of a doubler circuit realized with transistors having individual unity gain frequencies of 28 GHz.

9.8.2. Realization of the f_T -Doubler

A critical requirement underlying the optimal operation of the f_T -doubler in Fig. 9.47 is that transistors $M1$ and $M2$ conduct the same quiescent currents. This constraint stems primarily from the need to establish matched transconductances in the two utilized transistors. The traditional solution to the problem that no mechanism in the subject conceptual diagram assures requisite current mirroring is the modified doubler network depicted in Fig. 9.50.^[12] Note therein that any quiescent current, I_K , conducted by transistor $M1$, and hence by transistor $M3$ as well, is mirrored by transistor

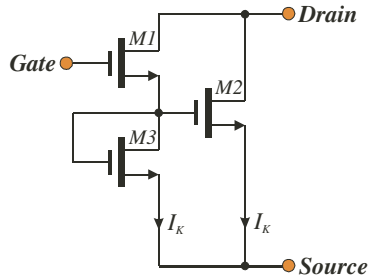


Figure 9.50. Doubler realization used to ensure that transistors $M1$ and $M2$ conduct nominally identical quiescent currents.

$M2$ if $M2$ and $M1$ are identical devices having matched gate aspect ratios. A drawback of the proposed compensation scheme is that the gate-source capacitance of transistor $M3$ is placed directly in shunt with the gate-source capacitance of $M2$, thereby incurring an effective doubling of the effective gate-source capacitance of the latter transistor. This shortcoming results in an f_T -doubler that actually delivers a unity gain frequency that is nominally only *1.5-times* larger than the unity gain frequency of either $M1$ or $M2$. A minor shortfall is the resistive load, whose approximate value is $1/g_m$, imposed on the gate-source terminals of $M2$ by the diode interconnection of transistor $M3$. In comparison to the native doubler of Fig. 9.47, this additional load serves to diminish, albeit slightly, the available short circuit current gain of the modified configuration.

9.9.0. Bandpass Feedback Amplifier

In contrast to the broadband architectures considered to this juncture, *band-pass, or narrowband, amplifiers* deliver gain only over a restricted signal passband that is geometrically apportioned about a *tuned, or center, frequency*. These bandpass structures are commonplace in a diversity of analog and digital communication systems. The receiver in these systems generally embodies an input, or *front-end*, linear amplifier to process audio, video, or digitally encoded information that is transmitted in the form of a modulated, fixed frequency carrier signal. This front-end amplifier, which is also typically referenced as a *radio frequency (RF) amplifier*, is invariably a bandpass structure satisfying several operational requirements.

In order to understand the salient aspects of the requisite properties of an RF amplifier, consider the abstraction posted in Fig. 9.51(a). The indicated

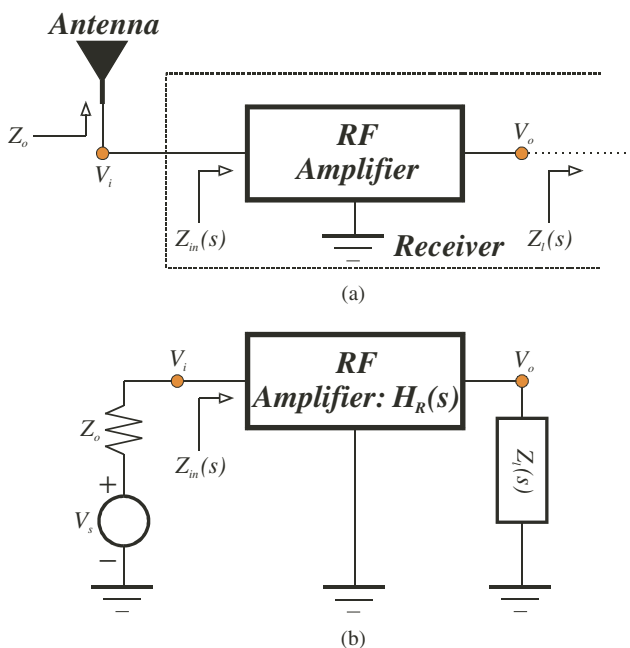


Figure 9.51. (a) Abstraction of the RF amplifier embedded in the front-end of a communications receiver. (b) Simplified electrical model of the system in (a).

RF amplifier is driven by an antenna that captures the modulated carrier signal. In narrowband communication systems, the frequency spectrum of this modulated carrier can be taken as embracing the frequency range, $(\omega_c \pm \omega_m/2)$, where ω_c is the radial value of the fixed carrier frequency, and ω_m is the radial value of the information passband. Since the antenna is a nominally linear entity, it can be represented as the Thévenin equivalent signal source depicted in Fig. 9.51(b). In the latter representation, V_s is the open circuit antenna voltage, and Z_o is the generally resistive characteristic impedance of the antenna, combined with the coupling medium that connects said antenna to the input port of the RF amplifier. The RF amplifier responds to the antenna excitation by delivering an output voltage, V_o , which can be related to V_s in the sinusoidal steady state through the transfer function,

$$H_R(j\omega) = \frac{V_o}{V_s} = \frac{H_o}{1 + jQ_o \left(\frac{\omega}{\omega_o} - \frac{\omega_o}{\omega} \right)}. \tag{9-164}$$

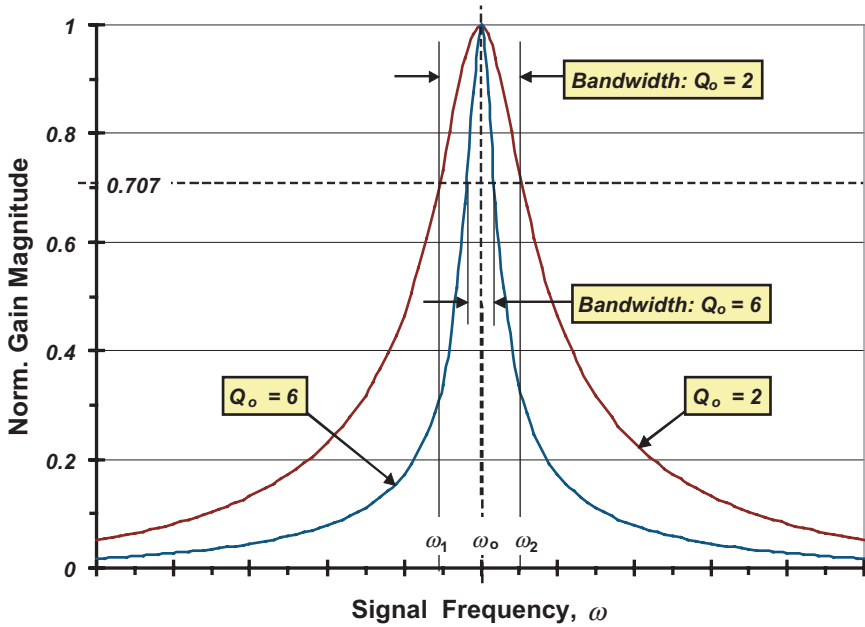


Figure 9.52. The generalized frequency response of an RF bandpass amplifier. The first order transfer function is given by Eq. (9-164). The 3-dB frequencies, ω_1 and ω_2 , are delineated for only the case of $Q_o = 2$.

In this expression, which embodies the net load impedance, Z_l , that terminates the amplifier output port, ω_o is the center frequency to which the RF amplifier is tuned, H_o , a constant, symbolizes the voltage gain observed at the tuned center frequency, and Q_o is the quality factor of the amplifier. Observe, as is highlighted by the normalized frequency response plot in Fig. 9.52, that for signal frequencies, ω , that are either far below or substantially above the center frequency, ω_o , the gain magnitude is considerably smaller than H_o . Moreover, the rate of gain attenuation increases dramatically with increases in the circuit quality factor, Q_o . These observations suggest that the amplifier center frequency, ω_o , should be tuned, or adjusted, to the transmitted carrier frequency, ω_c , to reduce the likelihood of amplifying potentially interfering signals transmitted by other communication channels whose carrier frequencies lie in the neighborhood of ω_c . Additionally, designs achieving relatively high Q_o are motivated, since progressively higher quality factors afford the RF amplifier the capability of effectively rejecting undesirable carrier frequencies that happen to

lie in the immediate neighborhood of ω_c . These contentions merely reflect the obvious desire that a radio tuned to a particular station or channel is expected to receive and process only the information emanating from the tuned station or channel, and not any information or data indigenous to another channel whose carrier frequency is proximate to that of the tuned station.

Equation (9-164) and its companion plots of Fig. 9.52 warrant further exploration with respect to the achievable bandwidth. Note the obvious fact that for any value of quality factor, the gain magnitude attenuates to 3-dB below the center frequency gain at precisely two signal frequencies. For the specific case of $Q_o = 2$ in Fig. 9.52, these frequencies are delineated as ω_1 and ω_2 . At either of these two frequencies, the magnitude of the j -term coefficient in the denominator on the right hand side of Eq. (9-164) must be one. Since $\omega_1 < \omega_o$, it follows that

$$Q_o \left(\frac{\omega_1}{\omega_o} - \frac{\omega_o}{\omega_1} \right) = -1, \quad (9-165)$$

while, since $\omega_2 > \omega_o$,

$$Q_o \left(\frac{\omega_2}{\omega_o} - \frac{\omega_o}{\omega_2} \right) = 1. \quad (9-166)$$

The respective solutions for the 3-dB frequencies in these two expressions are

$$\left. \begin{aligned} \omega_1 &= -\frac{\omega_o}{2Q_o} + \frac{\omega_o}{2Q_o} \sqrt{1 + 4Q_o^2} \\ \omega_2 &= +\frac{\omega_o}{2Q_o} + \frac{\omega_o}{2Q_o} \sqrt{1 + 4Q_o^2} \end{aligned} \right\}, \quad (9-167)$$

where it is understood that $|H_R(j\omega_1)| = |H_R(j\omega_2)| \equiv H_o/\sqrt{2}$. The 3-dB bandwidth, say, B_o , of the bandpass architecture is simply the difference between the foregoing 3-dB frequencies, whence

$$B_o = \omega_2 - \omega_1 = \frac{\omega_o}{Q_o}. \quad (9-168)$$

Since this bandwidth, which should be made at least as large as the information passband, ω_m , is inversely related to the circuit quality factor, Q_o , a progressively larger quality factor gives rise to an RF amplifier more sharply tuned to the center frequency, and thus an amplifier fully capable of discriminating between desired and most unwanted carriers. The signal discrimination attribute of large Q_o is also advantageous from an electrical

noise perspective. In particular, the total output noise precipitated by shot, flicker, and thermal processes generated within the amplifier is proportional to the amplifier bandwidth. It follows that design care should be exercised insofar as designing for an unnecessarily large value of 3-dB bandwidth.

A second noteworthy point is the observation from Eq. (9-167) that

$$\omega_o \equiv \sqrt{\omega_1 \omega_2}; \quad (9-169)$$

that is, the amplifier center frequency is the geometric mean of its two 3-dB frequencies. But for $2Q_o \gg 1$, which mathematically defines the *narrowband* case, Eq. (9-167) reduces, with the help of Eq. (9-168), to

$$\left. \begin{aligned} \omega_1 &\approx \omega_o - \frac{B_o}{2} \\ \omega_2 &\approx \omega_o + \frac{B_o}{2} \end{aligned} \right\}, \quad (9-170)$$

thereby inferring that for high Q_o , the amplifier center frequency approximates the arithmetic mean of its two 3-dB frequencies.

It is also important to appreciate the problems surrounding the fact that the Thévenin antenna voltage, V_s , is small in virtually all communication systems. Accordingly, the RF amplifier must satisfy three other fundamental design objectives, in addition to the basic requirement of sufficiently high gain at the tuned center frequency. The first of these is the desirability of ensuring that the amplifier input impedance, $Z_{in}(s)$, be matched to the antenna characteristic impedance, Z_o . This matching assures maximal signal power transfer between the antenna and the amplifier input port, thereby precluding unnecessary losses of unavoidably anemic signal power levels. But even with prevailing maximum power transfer conditions, there is a danger that the signal voltage associated with the actual power level observed at the amplifier input port may be so small as to be masked by the equivalent input noise voltage of the amplifier. To ensure sufficiently low equivalent input noise, design care must therefore be exercised with respect to the choice of amplifier topology, biasing of the active elements implicit to the selected topology, and the prudent use of inherently noisy passive resistances in the critical signal flow paths of the amplifier. Finally, the age of portable electronics demands that the RF amplifier be capable of operating optimally with low standby power requirements. Unfortunately, low power design objectives often run counter to the requirements of impedance matching, low noise, and high center frequency gain.^[13]

9.9.1. Common Source RF Amplifier

Although the literature is rife with viable RF amplifiers, the topology currently favored in the state of the art is the low power, low voltage configuration depicted schematically in Fig. 9.53(a). In this structure, transadmittance feedback in the form of the source lead inductance, $L_{s,s}$, is exploited as an ideally lossless vehicle for achieving the desired matching between

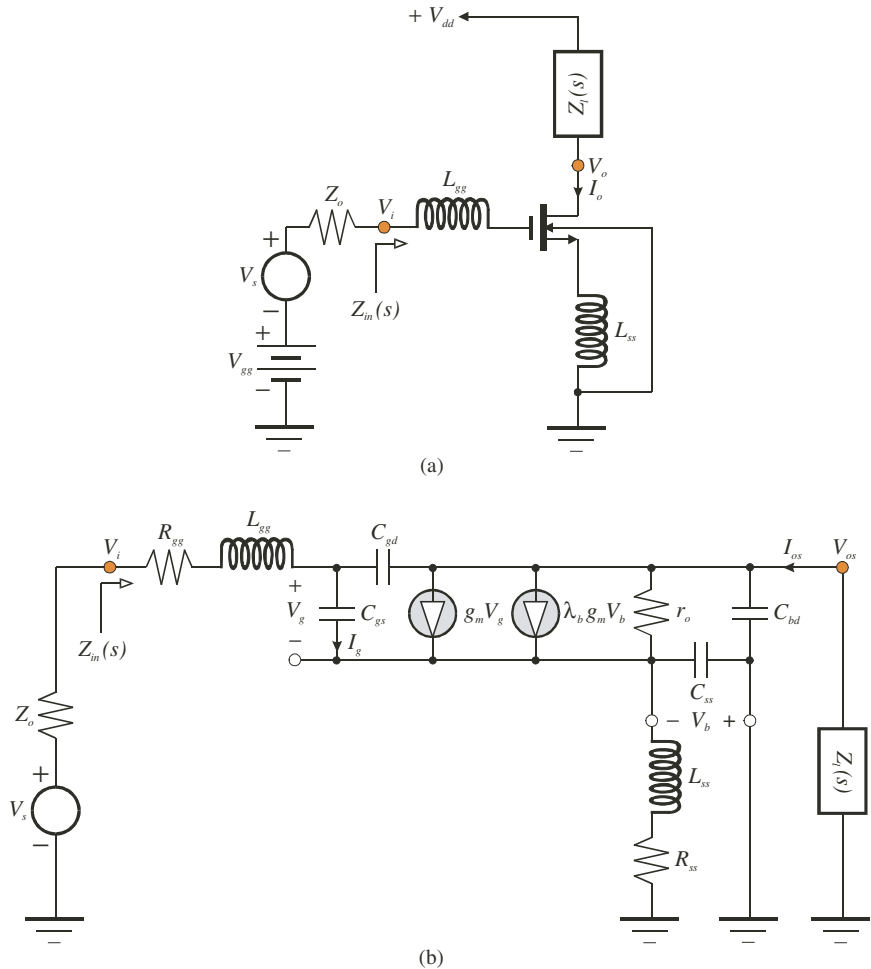


Figure 9.53. (a) The basic schematic diagram of a low voltage, low power RF amplifier realized in MOS technology. The transistor is biased in saturation. (b) High frequency, small signal equivalent circuit of the amplifier in (a).

the driving point input impedance, $Z_{in}(s)$, and the Thévenin signal source resistance, Z_o , at the tuned center frequency, ω_o , of the amplifier. Specifically, L_{ss} can be chosen to ensure $Z_{in}(j\omega_o) = Z_o$, where frequency ω_o is determined by the resonant interaction of the net gate lead inductance and the net effective input capacitance of the amplifier stage. Because only inductive impedances are exploited in both the source and the gate leads of the transistor, low power, low voltage biasing is facilitated, since within the ivy-cloaked halls of academe, inductors are lossless circuit elements. As is demonstrated shortly, the indicated load impedance, $Z_l(s)$, like the source lead impedance, must be dominantly inductive over the RF amplifier passband.

Recalling the modeling disclosures in *Chapter 7*, the pertinent small signal model of the RF amplifier is the network in Fig. 9.53(b). In this model, R_{ss} symbolizes the resistance implicit to the integrated circuit metallization spiral that forges inductance L_{ss} , while capacitance C_{ss} accounts for transistor bulk-source capacitance, the capacitance precipitated between the spiral metallization and inductor interconnect wiring crossing under the individual spiral segments, and the capacitance evidenced between signal ground and the top layer metallization winding.^[14] Since the gate lead inductance, L_{gg} , can be synthesized with bond wire, no effort is expended to model the parasitic capacitance associated with this element. Although the quality factor of bond wire inductances is typically large, a resistance, R_{gg} , is nonetheless included in series connection with L_{gg} . The remaining modeling elements in the figure are those that are traditionally considered in high frequency representations of the small signal behavior of MOS technology devices.

Before attempting a definitive analysis of the subject RF amplifier, the model in Fig. 9.53(b) can be sanitized in concert with a few reasonable approximations and basic circuit theoretic principles. To wit, bulk-induced threshold voltage modulation can be ignored, assuming that at the amplifier center frequency, the controlled current, $\lambda_b g_m V_b$ is much smaller than the primary controlled current, $g_m V_g$. Accordingly, λ_b , which is a measure of said threshold phenomena, is set to zero. Second, the channel resistance, r_o , is presumed large enough to justify its neglect. In truth, r_o may be only a few thousand ohms in deep submicron MOS technology devices, but it is nevertheless likely that r_o substantially exceeds the magnitude, $|Z_l(j\omega_o)|$, of the load impedance at the amplifier center frequency. Third, the bulk-drain capacitance, C_{bd} , of the transistor can be conveniently absorbed into the terminating load impedance, which may include capacitive phenomena

associated with inductances embedded in the drain circuit. Fourth, the transistor gate-drain capacitance, C_{gd} , is presumed small, but not necessarily negligible, particularly with respect to the delineation of the amplifier driving point input impedance. The presumption of small gate-drain capacitance requires the use of self-aligned gate technology processing and/or the incorporation of a common gate cascode between the load impedance and the drain of the degenerated common source amplifier. Finally, because considerable interest focuses on the evaluation of the driving point input impedance, which entails that the effective impedance in the transistor source terminal be referred to its gate lead, it is convenient to transform the voltage controlled current source, $g_m V_g$, into an equivalent current controlled element. To the latter end, Fig. 9.53(b) projects

$$g_m V_g = g_m \left(\frac{I_g}{sC_{gs}} \right) = \left(\frac{k_g \omega_T}{s} \right) I_g, \tag{9-171}$$

where Eq. (9-158) is used, I_g is the indicated signal current conducted by the transistor gate-source capacitance, C_{gs} , and

$$k_g \triangleq 1 + \frac{C_{gd}}{C_{gs}}. \tag{9-172}$$

The resultantly simplified model is shown in Fig. 9.54.

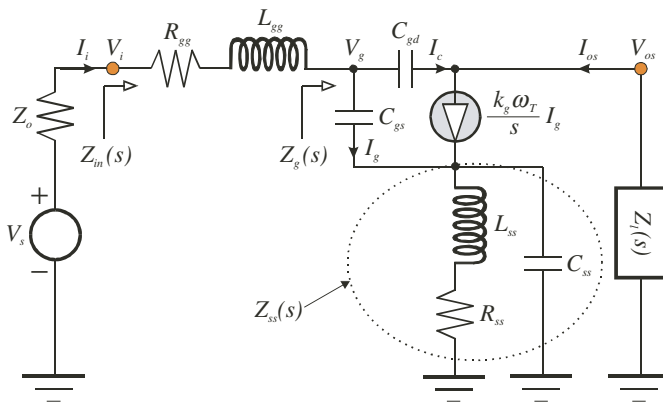


Figure 9.54. Simplified small signal, high frequency model of the RF amplifier shown in Fig. 9.53(a).

9.9.2. Impedance and Transfer Characteristics

It is a simple matter to show that the source circuit impedance indicated as $Z_{ss}(s)$ in Fig. 9.54 is given analytically by

$$Z_{ss}(s) = \frac{R_{ss} \left(1 + \frac{Q_s s}{\omega_s} \right)}{1 + \frac{s}{Q_s \omega_s} + \left(\frac{s}{\omega_s} \right)^2}, \quad (9-173)$$

where

$$\omega_s = \frac{1}{\sqrt{L_{ss} C_{ss}}} \quad (9-174)$$

is the undamped natural, or self-resonant, frequency of the inductance inserted into the source lead of the transistor. Moreover,

$$Q_s = \frac{\omega_s L_{ss}}{R_{ss}} = \frac{1}{R_{ss}} \sqrt{\frac{L_{ss}}{C_{ss}}} \quad (9-175)$$

defines the quality factor of the source lead inductance at the aforementioned self-resonant frequency. It is important to underscore that ω_s is *not* the tuned center frequency, ω_o , of the amplifier undergoing investigation. Indeed, ω_s must be significantly larger than ω_o if the amplifier is to function properly in the sense of an *I/O* performance that is nominally insensitive to the net capacitance incident between signal ground and the source lead of the transistor. Ideally, $\omega_s = \infty$, which for finite inductance L_{ss} , demands the physically unachievable circumstance of $C_{ss} = 0$. In lieu of $\omega_s = \infty$, large ω_s is manifested by assiduously laying out the on chip spiral inductor to minimize its parasitic capacitances.^[15,16] Additionally, a minimal geometry transistor can be used to avoid unduly large bulk-source capacitance and/or consideration can be given to connecting together bulk and source terminals. As usual, care must be exercised to preclude substrate current conduction when the bulk is connected to the source, particularly since in the circuit at hand, the inductive impedance in the transistor source lead can be large at high signal frequencies. In the limit of very large ω_s , Eq. (9-175) reduces Eq. (9-173) to the expected result,

$$Z_{ss}(s) \approx R_{ss} + sL_{ss}. \quad (9-176)$$

The driving point input impedance, $Z_{in}(s)$, of the RF amplifier modeled in Fig. 9.54 is obviously

$$Z_{in}(s) = \frac{V_i}{I_i} = R_{gg} + sL_{gg} + Z_g(s), \quad (9-177)$$

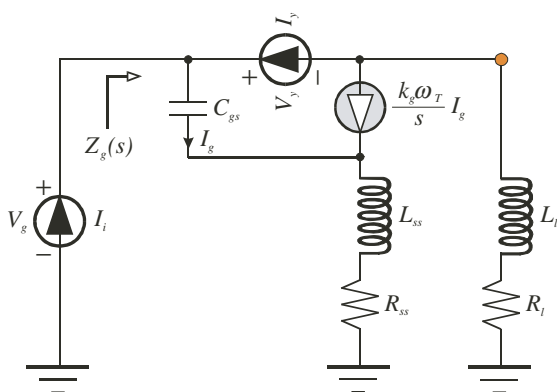


Figure 9.55. Small signal equivalent circuit for applying signal flow analysis techniques to the evaluation of the impedance, $Z_g(s)$, in Fig. 9.54.

where, in terms of the current, I_g , and the voltage, V_g , delineated in the diagram, the impedance, $Z_g(s)$, seen looking directly into the gate terminal of the transistor utilized in the amplifier is

$$Z_g(s) = \frac{V_g}{I_i} \tag{9-178}$$

9.9.2.1. Gate Impedance

The gate terminal impedance identified by Eq. (9-178) is best evaluated with the signal flow analytical techniques developed in a preceding chapter. Unfortunately, the formulation of a useful expression for this impedance in terms of any general load termination, $Z_l(s)$, is a challenging, if not impossible, task. The determination of the subject gate impedance begins by assuming for the moment that $Z_l(s)$ is the simple inductive impedance,

$$Z_l(s) = R_l + sL_l, \tag{9-179}$$

where R_l is the presumably small resistance associated with the coil that forges inductance L_l . In advance of a discussion focused on the logistics of this particular selection of load impedance termination, Fig. 9.55 delineates the small signal model pertinent to a signal flow evaluation of the gate impedance of interest. In particular, $Z_g(s)$ can be expressed in the form,

$$Z_g(s) = \frac{V_g}{I_i} = Z_{go}(s) \left(\frac{1 + sC_{gd}Z_{qr}}{1 + sC_{gd}Z_{qs}} \right), \tag{9-180}$$

where $Z_{go}(s)$ is the input impedance when C_{gd} is tacitly ignored or equivalently, when $I_y = 0$; that is,

$$Z_{go}(s) = \left. \frac{V_g}{I_i} \right|_{I_y=0}. \quad (9-181)$$

By inspection of the model at hand, $Z_{go}(0)$ is noted to be infinitely large, thereby constraining the validity of Eq. (9-180) to only nonzero signal frequencies. This disclaimer hardly comprises a practical restriction since attention to the RF amplifier undergoing study is directed to signal frequencies lying in the neighborhood of the generally high tuned center frequency of the circuit. The parameter, Z_{qs} , in Eq. (9-180) is the normalized return ratio with respect to the capacitive admittance, sC_{gd} . It is literally the impedance facing capacitor C_{gd} under the condition of an open circuited gate port, so that

$$Z_{qs} = \left. \frac{V_y}{I_y} \right|_{I_i=0}. \quad (9-181)$$

On the other hand, the impedance function, Z_{qr} , is the normalized null return ratio with respect to admittance sC_{gd} . It is evaluated under the condition of a short circuited gate port in accordance with

$$Z_{qr} = \left. \frac{V_y}{I_y} \right|_{V_g=0}. \quad (9-182)$$

An inspection of the model in Fig. 9.55 reveals that when current I_y is set to zero,

$$V_g = \left(\frac{1}{sC_{gs}} \right) I_i + (R_{ss} + sL_{ss}) \left(1 + \frac{k_g \omega_T}{s} \right) I_i. \quad (9-183)$$

It follows that $Z_{go}(s)$ is the impedance of a series RLC circuit in that

$$Z_{go}(s) = \left. \frac{V_g}{I_i} \right|_{I_y=0} = R_g + sL_{ss} + \frac{1}{sC_g}, \quad (9-184)$$

where

$$R_g = R_{ss} + k_g \omega_T L_{ss} \approx k_g \omega_T L_{ss} \quad (9-185)$$

and, recalling Eqs. (9-158) and (9-172),

$$C_g = \frac{C_{gs}}{1 + k_g \omega_T R_{ss} C_{gs}} = \frac{C_{gs}}{1 + g_m R_{ss}} \approx C_{gs}. \quad (9-186)$$

The approximations invoked in the preceding two relationships reflect the fact that the resistance, R_{ss} , associated with the commonly small source degeneration inductance, L_{ss} , is typically very small.

Observe that if current I_y is zero, which is closely approximated if C_{gd} is a negligibly small device capacitance, $Z_g(s)$ in Eq. (9-180) is precisely given by the right hand side of Eq. (9-184). It follows that when this V_g/I_i ratio is inserted into the input impedance expression of Eq. (9-177), an impedance match to a purely resistive source termination can be accomplished by choosing inductance L_{ss} correctly. The resultant series combination of this inductance and the gate lead inductance, L_{gg} , can then be made to resonate with capacitance C_g at the tuned center frequency of the amplifier. The significance of these observations is that the input resistance commensurate with maximum power transfer at the RF amplifier input port is realized at the amplifier center frequency in a nominally lossless fashion through the inductance, L_{ss} . In contrast, a desired input resistance realized straightforwardly as a resistive shunt across the amplifier input port incurs potentially unacceptable power dissipation.

Yet another advantage accrues from tuning the input port of the RF amplifier. In particular, only those signal currents whose frequencies lie in the immediate neighborhood of the tuned center frequency are predominantly conducted to the gate terminal of the transistor. On the other hand, currents whose frequencies lie appreciably outside the amplifier passband are substantially attenuated, as noted earlier in the general discussion of tuned circuits. It follows that any electrical noise detected as interfering energy at the antenna site is largely precluded from contaminating the signal processing capabilities of the transistor, and hence the amplifier response, provided that the power spectral density of the detected noise lies outside the amplifier passband. In short, the total output noise of an amplifier is nominally proportional to the circuit bandwidth. Accordingly, narrowbanding the input port shields the transistor from contaminating noise energy and serves to reduce the total output noise of the RF amplifier.

Continuing with the analysis, it can be demonstrated that

$$Z_{qs} = \left. \frac{V_y}{I_y} \right|_{I_i=0} = Z_{go}(s) + R_l + k_g \omega_T L_l + sL_l + \frac{k_g \omega_T R_l}{s}, \quad (9-187)$$

and

$$Z_{qr} = \left. \frac{V_y}{I_y} \right|_{V_g=0} = R_l + sL_l. \quad (9-188)$$

The substitution of Eqs. (9-187) and (9-188) into Eq. (9-180) produces

$$Z_g(s) = Z_{go}(s) \left(\frac{1 + sR_l C_{gd} + s^2 L_l C_{gd}}{1 + k_g \omega_T L_l C_{gd} + s Z_{go}(s) C_{gd} + s(R_l + k_g \omega_T L_l) C_{gd} + s^2 L_l C_{gd}} \right). \quad (9-189)$$

It is more convenient to deal with the admittance, $Y_g(s)$, corresponding to impedance $Z_g(s)$, whereupon Eq. (9-189) is seen to imply

$$Y_g(s) = Y_{go}(s) \times \left\{ 1 + \frac{k_g \omega_T R_l C_{gd} + s[k_g \omega_T L_l C_{gd} + Z_{go}(s) C_{gd}]}{1 + sR_l C_{gd} + s^2 L_l C_{gd}} \right\}, \quad (9-190)$$

where, of course,

$$Y_{go}(s) = \frac{1}{Z_{go}(s)} = \frac{sC_g}{1 + sR_g C_g + s^2 L_{ss} C_g}. \quad (9-191)$$

The algebraic complexity of Eq. (9-190) encourages a loudly tolling bell for suitable approximations. To this end, recall that for the ideal circumstance of $C_{gd} = 0$, the impedance seen looking directly into the gate terminal is simply $Z_{go}(s)$ or equivalently, the gate terminal admittance is $Y_{go}(s)$. While null C_{gd} is a dubious presumption for high frequency signal processing, small C_{gd} is a prudent analytical tack, particularly if the utilized transistor derives from a self-aligned gate process. If, in addition to small C_{gd} , R_l assumes its expected small value, the magnitudes of the critical frequencies associated with the terms in $sR_l C_{gd}$ and $s^2 L_l C_{gd}$ in the denominator of the second term on the right hand side of Eq. (9-190) can be presumed to be far larger than the tuned center frequency, ω_o , of the amplifier. Accordingly, Eq. (9-190) reduces to

$$Y_g(s) \approx Y_{go}(s) + sC_{gd} + \left[\frac{sk_g \omega_T R_l C_{gd} C_g + s^2 k_g \omega_T L_l C_{gd} C_g}{1 + sR_g C_g + s^2 L_{ss} C_g} \right]. \quad (9-192)$$

The last expression suggests that the admittance seen looking into the gate terminal of the transistor in the RF amplifier under consideration is comprised of a shunt interconnection of three distinct electrical branches. Unfortunately, the bracketed term on the far right hand side of Eq. (9-192) defies a positive real circuit interpretation. Indeed, the presence of the s^2 -term in the numerator of this bracketed quantity even gives rise to a possible negative branch element resistance in the extreme (and impractical)

situation of large gate-drain capacitance and/or large drain circuit inductance. In an attempt to facilitate a pragmatic design strategy, the term in $s^2 L_{ss} C_g$ can be neglected for most RF amplifier designs. Moreover, the frequency associated with the time constant, $R_g C_g$, is invariably much larger than the tuned center frequency of the amplifier, if said center frequency is smaller than the unity gain frequency of the utilized transistor by a factor of at least 20. Using Eqs. (9-158), (9-172), and (9-186), the foregoing observations allow Eq. (9-192) to be collapsed further to the first order result,

$$Y_g(s) \approx Y_{go}(s) + sC_m, \quad (9-193)$$

where “Miller time” is apparent through the defining capacitance,

$$C_m \triangleq \left(1 + \frac{g_m R_l}{1 + g_m R_{ss}} \right) C_{gd}. \quad (9-194)$$

The Miller multiplier in Eq. (9-196) differs from the traditionally encountered factor, $(1 + g_m R_l)$, because at low signal frequencies, the forward transconductance, g_m , of the transistor is degenerated by an amount of $(1 + g_m R_{ss})$ due to the source terminal resistance, R_{ss} . At this juncture, Eqs. (9-184) and (9-193) combine to forge the high frequency modeling approximation advanced in Fig. 9.56(a).

Two additional modeling tasks remain. The first involves rendering the model in Fig. 9.56(a) more analytically convenient by couching a dependence of the indicated current controlled current source on the net input current, I_i , as opposed to a direct dependence on the gate-source capacitance current, I_g . To this end, a simple current divider gives rise to

$$\frac{I_g}{I_i} = \frac{sC_g}{sC_g + sC_m (1 + sR_g C_g + s^2 L_{ss} C_g)} \approx \frac{C_g}{C_g + C_m}, \quad (9-195)$$

where the approximation reflects the recurring presumption that the critical frequencies, $1/R_g C_g$ and $1/\sqrt{L_{ss} C_g}$, are significantly larger than the tuned center frequency of the amplifier. The second of the aforementioned two modeling tasks is the reduction of the input port circuit in Fig. 9.56(a) to the simple series impedance interconnection promoted by Fig. 9.56(b). To this end, Eq. (9-193), the critical frequency assumptions invoked to arrive at Eq. (9-195), and Fig. 9.56(a) combine to deliver an effective series input

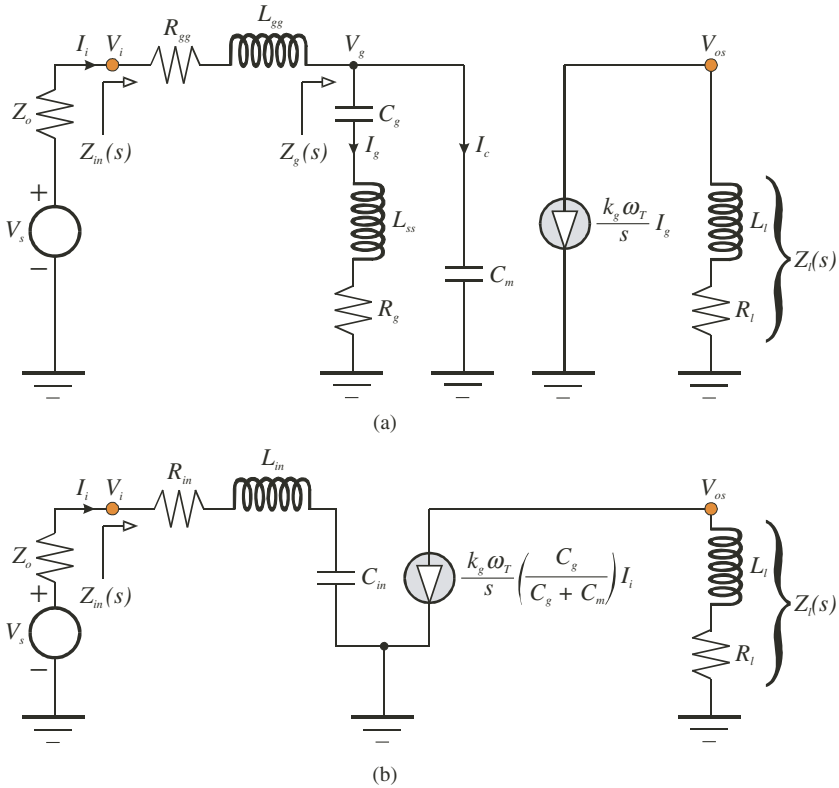


Figure 9.56. (a) The approximate high frequency model of the RF amplifier considered in Fig. 9.53(a). (b) Alternative form of the equivalent circuit in (a).

resistance, R_{in} , of

$$R_{in} = R_{gg} + \left(\frac{C_g}{C_g + C_m} \right) R_g \approx R_{gg} + \left\{ \frac{C_{gs}}{C_{gs} + [1 + g_m (R_{ss} + R_l)] C_{gd}} \right\} \times (R_{ss} + k_g \omega_T L_{ss}), \tag{9-196}$$

an effective series input port inductance, L_{in} , of

$$L_{in} = L_{gg} + \left(\frac{C_g}{C_g + C_m} \right) L_{ss} \approx L_{gg} + \left\{ \frac{C_{gs}}{C_{gs} + [1 + g_m (R_{ss} + R_l)] C_{gd}} \right\} L_{ss}, \tag{9-197}$$

and an effective series input port capacitance, C_{in} , of

$$C_{in} = C_g + C_m \approx \frac{C_{gs}}{1 + g_m R_{ss}} + \left(1 + \frac{g_m R_l}{1 + g_m R_{ss}}\right) C_{gd}. \quad (9-198)$$

An inspection of Eq. (9-196) reveals that impedance matching to the Thévenin source resistance, Z_o , shown in Fig. 9.56(b) can be effected at the tuned center frequency, ω_o , if inductance L_{in} resonates with capacitance C_{in} at radial frequency ω_o and if L_{ss} is selected to deliver $R_{in} = Z_o$. Thus,

$$\omega_o = \frac{1}{\sqrt{L_{in} C_{in}}}, \quad (9-199)$$

and

$$R_{in} = Z_o = R_{gg} + \left\{ \frac{C_{gs}}{C_{gs} + [1 + g_m (R_{ss} + R_l)] C_{gd}} \right\} R_g, \quad (9-200)$$

where R_g remains given by Eq. (9-185). Equations (9-199) and (9-200) now allow the driving point input impedance to be formulated as

$$Z_{in}(j\omega) \approx Z_o + j\omega_o L_{in} \left(\frac{\omega}{\omega_o} - \frac{\omega_o}{\omega} \right), \quad (9-201)$$

which analytically substantiates $Z_{in}(j\omega_o) \approx Z_o$.

Before proceeding further, it is wise to interject a word of engineering caution as regards the propriety of Eqs. (9-195) through (9-198) and (9-200). In particular, all of these expressions are predicated on crude, first order approximations invoked on Eq. (9-192). The errors potentially resulting from these approximations are best explained by returning to the basic impedance relationship of Eq. (9-180). In this relationship, it should be understood that capacitance C_{gd} is inherently very small in any MOSFET deemed viable for incorporation into a high performance RF amplifier. In the neighborhood of the tuned center frequency, it follows that the magnitudes of the numerator and denominator within the parenthesized term on the right hand side of Eq. (9-180) are respectively very nearly unity. In addition to near unity magnitudes, the phasor angles of these numerator and denominator quantities are invariably very small near the amplifier center frequency. Thus, the real part of impedance $Z_g(j\omega_o)$, to which the real part of the amplifier driving point input impedance is intimately related, is dependent on the cosine of a difference of two very small angles, which begets potentially large computational errors unless the individual numerator and denominator angles are accurately determined. This inherent problem of analytical accuracy is exacerbated by the fact that in general,

$Z_{go}(j\omega_o)$ is strongly capacitive, which portends an impedance angle in the range -80° to -90° . Since the real part of the input impedance is linearly related to the cosine of an angle that equals the sum of the angle of $Z_{go}(j\omega_o)$ and the aforementioned difference angle between the numerator and denominator terms in Eq. (9-180), a potentially large computational error can be rightfully anticipated. For example, there is a difference of almost 25% between the cosine of (-82°) and the cosine of (-84°) . It is entirely inappropriate to presume tacitly that the approximations invoked herewith imply an impedance angle accuracy of $\pm 10^\circ$, yet alone a $\pm 2^\circ$ precision.

The foregoing disclaimer does not infer that the equations noted above have zero engineering value. Indeed, the relationships are worthy of the paper that espouses them, for they offer the designer a means of computing first order values for relevant circuit elements. Armed with these first order parameter estimations, a design optimization can be executed on MATLAB, EXCEL, or suitable other software to discern final values for all designable circuit elements. Implicit to this design optimization tack is the fact that $Z_g(j\omega)$ in Eq. (9-180), and hence $Z_{in}(j\omega)$ in Eq. (9-177), can be programmed as a function of the radial signal frequency, ω , and all resistive, capacitive, and inductive elements of the amplifier model. A methodically manual, or even semi-automated, adjustment in the inductances, L_{ss} , L_{gg} , and L_l , can then be pursued to arrive at the optimal design solution.

9.9.2.2. Voltage Transfer Function

The analyses and associated approximations that deliver the simplified high frequency equivalent circuit offered in Fig. 9.56(b) produce an input port signal current, I_i , of

$$I_i(j\omega) = \frac{V_s(j\omega)}{Z_o + Z_{in}(j\omega)} = \frac{V_s(j\omega)}{Z_o + Z_o + j\omega L_{in} + \frac{1}{j\omega C_{in}}}, \quad (9-202)$$

or

$$I_i(j\omega) = \frac{V_s(j\omega)/2Z_o}{1 + jQ_o\left(\frac{\omega}{\omega_o} - \frac{\omega_o}{\omega}\right)}, \quad (9-203)$$

where in terms of center frequency ω_o and 3-dB bandwidth B_o ,

$$Q_o = \frac{\omega_o}{B_o} = \frac{\omega_o L_{in}}{2Z_o} = \frac{1}{2Z_o} \sqrt{\frac{L_{in}}{C_{in}}}. \quad (9-204)$$

The voltage transfer function, $H_R(j\omega)$, of the RF amplifier now follows directly from Fig. 9.56(b) and Eq. (9-203). In particular,

$$\begin{aligned} H_R(j\omega) &= \frac{V_{os}(j\omega)}{V_s(j\omega)} = \frac{V_{os}(j\omega)}{I_i(j\omega)} \times \frac{I_i(j\omega)}{V_s(j\omega)} \\ &= -\frac{\left(\frac{k_g\omega_T}{j\omega}\right)\left(\frac{C_g}{C_g + C_m}\right)\left[\frac{Z_l(j\omega)}{2Z_o}\right]}{1 + jQ_o\left(\frac{\omega}{\omega_o} - \frac{\omega_o}{\omega}\right)}. \end{aligned} \quad (9-205)$$

This result is similar to the desired transfer function form of Eq. (9-164), with the notable exception that the numerator on the right hand side of Eq. (9-205) is not frequency invariant, as is the constant signified by parameter H_o in Eq. (9-164). The problem at hand is circumvented if the terminating load is the impedance, $Z_l(j\omega) = j\omega L_l$, of an ideal inductance, L_l . In such a circumstance, Eq. (9-205) emulates Eq. (9-164) in the sense that H_o is rendered frequency invariant. Specifically,

$$\begin{aligned} H_R(j\omega_o) &\triangleq H_o = -k_g \left(\frac{C_g}{C_g + C_m}\right) \left(\frac{\omega_T L_l}{2Z_o}\right) \\ &= -k_g \left(\frac{C_g}{C_g + C_m}\right) Q_o \left(\frac{\omega_T}{\omega_o}\right) \left(\frac{L_l}{L_{in}}\right), \end{aligned} \quad (9-206)$$

where Eq. (9-204) is exploited.

Unfortunately, the realization of the drain circuit load impedance, $Z_l(s)$, as an ideal inductance, L_l , comprises engineering fantasy. Any attempt to incorporate an inductor into this drain circuit unavoidably incurs parasitic series resistance and shunt capacitance and results in an inductive subcircuit that is topologically identical to the subcircuit associated with the source terminal inductance, L_{ss} . This contention is highlighted in Fig. 9.57, where L_l is understood to be the desired drain circuit inductance, R_l is the series resistance associated with said inductance, and C_l embodies parasitic load capacitance at the output port, transistor bulk-drain capacitance, and the capacitance associated with the realization of inductance L_l . Because the network defining $Z_l(s)$ in Fig. 9.57 is topologically identical to that which defines impedance $Z_{ss}(s)$ in the same figure, Eqs. (9-173) through (9-175) can be adapted to write for $Z_l(s)$,

$$Z_l(s) = \frac{R_l \left(1 + \frac{sQ_l}{\omega_o}\right)}{1 + \frac{sx}{Q_l\omega_o} + \left(\frac{s}{\omega_o}\right)^2 x} = \frac{sL_l \left(1 + \frac{\omega_o}{Q_l s}\right)}{1 + \frac{sx}{Q_l\omega_o} + \left(\frac{s}{\omega_o}\right)^2 x}, \quad (9-207)$$

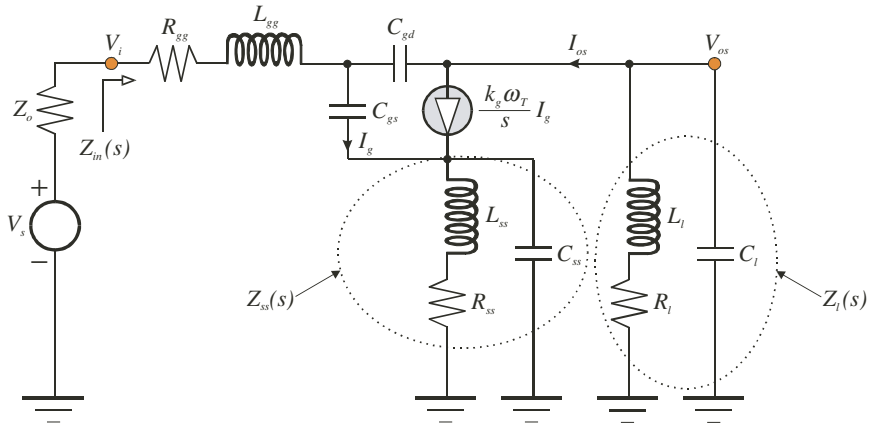


Figure 9.57. The high frequency model of the RF amplifier in Fig. 9.53(a) with the drain circuit load impedance realized as a practical circuit integrated circuit inductor.

where ω_o is the amplifier center frequency defined by Eq. (9-199),

$$Q_l = \frac{\omega_o L_l}{R_l}, \tag{9-208}$$

is the quality factor of the load circuit inductance measured at the amplifier center frequency, and parameter x is

$$x = \omega_o^2 L_l C_l. \tag{9-209}$$

Note that x represents little more than the inverse square of the self-resonant frequency of the load circuit inductance, normalized to the tuned center frequency. Clearly, if $x \ll 1$ and $Q_l \gg 1$, the impedance given as Eq. (9-207) approximates the desired ideal load circuit inductance, at least in the neighborhood of frequency ω_o . The requirement, $x \ll 1$, imposes a limit on the allowable load circuit capacitance, while the objective of a very large load quality factor can be met easily if the drain circuit inductance is realized as a bond wire connecting the transistor drain terminal to the positive circuit supply voltage.

Example 9.8. When operated from a 50 ohm signal source, the bandpass amplifier of Fig. 9.53(a) is to be designed to deliver a voltage gain magnitude of five (14 dB) at a tuned center frequency of 1900 MHz and a 3-dB bandwidth of 360 MHz. The transistor utilized in the amplifier is appropriately biased in saturation where it has a short circuit unity gain frequency of 42 GHz, a drain-source channel resistance of 10 K Ω , and a bulk-induced threshold modulation factor of 0.03. For the

given MOSFET process, the gate-drain capacitance is known to be roughly 2.5% of the gate-source capacitance. Assume that the source and drain circuit inductances are realized as on chip spirals having a nominal quality factor of no more than 9 at 1900 MHz. On the other hand, the gate circuit inductance is to be implemented either with bond wire or as an off chip element and has a nominal quality factor of 40 at the tuned center frequency of the amplifier. Design the network by calculating all requisite inductances and stipulating the maximum allowable capacitive loading at both the source and drain terminals of the transistor. Use HSPICE to simulate the small signal response of the designed amplifier, using the small signal model shown in Fig. 9.53(b).

Solution 9.8.

- (1) From Eq. (9-168), a 3-dB bandwidth of $B_o = 2\pi(360 \text{ MHz})$ and a center frequency of $\omega_o = 2\pi(1900 \text{ MHz})$ requires a circuit quality factor of $Q_o = 5.278$. Since $Z_o = 50 \Omega$, Eq. (9-204) stipulates a net input circuit inductance of $L_{in} = 44.21 \text{ nH}$. In Eq. (9-199), the requisite net input capacitance corresponding to $\omega_o = 2\pi(1900 \text{ MHz})$ is $C_{in} = 158.7 \text{ fF}$. Thus, an effective input inductance of $L_{in} = 44.21 \text{ nH}$ establishes the circuit quality factor ($Q_o = 5.278$) appropriate to the bandwidth design target of $B_o = 360 \text{ MHz}$. In tandem with this inductance requirement, a net effective input capacitance of $C_{in} = 158.7 \text{ fF}$ sets the amplifier center frequency, about which the aforementioned bandwidth is centered, to the design goal of $\omega_o = 2\pi(1900 \text{ MHz})$.
- (2) In an attempt to maximize the accuracy of relevant design computations, it is necessary to estimate values for the parasitic resistances, R_{gg} , R_{ss} , and R_l , associated respectively with circuit inductances L_{gg} , L_{ss} , and L_l . One way of accomplishing this feat is to predicate first order values of all circuit inductances on the tacit assumption of negligible parasitic resistances. Once these first order inductance values are available, the subject resistances can be estimated from the stipulated quality factors of the inductances. Inductances can then be reevaluated to arrive at their respective initial design values by accounting for the estimated resistances in the appropriate design equations. This procedure obviously results in finalized inductance quality factors that differ somewhat from their nominal specifications. This variance is acceptable in light of the fact that quality factors are not mere constants, but are actually intricate functions of frequency and numerous physical parameters. Accordingly, the quality factors provided in the problem statement should be viewed as only reasonable estimates of actual performance metrics related to inductor losses.

Since $C_{gd} = 0.025C_{gs}$, k_g in Eq. (9-172) is $k_g = 1.025$. With parasitic resistances ignored, Eq. (9-200) yields

$$Z_o \approx \left(\frac{C_{gs}}{C_{gs} + C_{gd}} \right) k_g \omega_T L_{ss} = \left(\frac{1}{k_g} \right) k_g \omega_T L_{ss} = \omega_T L_{ss}, \quad (\text{E8-1})$$

where Eq. (9-172) has been applied. For $Z_o = 50 \Omega$ and $\omega_T = 2\pi(42 \text{ GHz})$, the preliminary value of source circuit inductance L_{ss} is 189.5 pH. Given a nominal inductor quality factor of 9 at the amplifier center frequency, $R_{ss} = \omega_o L_{ss}/9 = 0.2513 \Omega$. Conservatism is arguably prudent in bandpass high frequency amplifier designs and thus, R_{ss} might be increased by some 10% to a value of $R_{ss} = 0.275 \Omega$.

Continuing with the tacit neglect of inductor resistances, Eq. (9-197) provides

$$L_{in} \approx L_{gg} + \frac{L_{ss}}{k_g}, \quad (\text{E8-2})$$

and with $L_{in} = 44.21 \text{ nH}$, $L_{ss} = 189.5 \text{ pH}$, and $k_g = 1.025$, $L_{gg} = 44.02 \text{ nH}$. Since the quality factor of the gate inductance is roughly 40 at $\omega = \omega_o$, R_{gg} follows as $R_{gg} = \omega_o L_{gg}/40 = 13.14 \Omega$. As with the adjustment to R_{ss} above, increase this resistance value by approximately 10% to $R_{gg} = 14.5 \Omega$.

Using Eq. (9-198), the input capacitance can be approximated as

$$C_{in} \approx C_{gs} + C_{gd} = k_g C_{gs}. \quad (\text{E8-3})$$

Since $C_{in} = 158.7 \text{ fF}$ and $k_g = 1.025$, $C_{gs} = 154.8 \text{ fF}$, whence $C_{gd} = 0.025 C_{gs} = 3.871 \text{ fF}$. Accordingly, $\omega_T = 2\pi(42 \text{ GHz})$ in Eq. (9-158) requires transistor biasing and geometry commensurate with a forward transconductance of $g_m = 41.88 \text{ mmho}$.

Continuing with the approximations invoked thus far, the ratio, $[C_g/(C_g + C_m)]$, approximates $1/k_g$ so that the center frequency voltage gain relationship in Eq. (9-206) becomes

$$H_o \approx Q_o \left(\frac{\omega_T}{\omega_o} \right) \left(\frac{L_l}{L_{in}} \right). \quad (\text{E8-4})$$

For $Q_o = 5.278$, $\omega_T = 2\pi(42 \text{ GHz})$, $\omega_o = 2\pi(1900 \text{ MHz})$, and $L_{in} = 44.21 \text{ nH}$, a gain magnitude of $|H_o| = 5$, is seen to require a drain circuit inductance of $L_l = 1.895 \text{ nH}$. With an inductance quality factor of 9, this inductance implies a series parasitic resistance of $R_l = 2.513 \Omega$. Design conservatism beckons an increase of this estimated inductor resistance to $R_l = 2.75 \Omega$.

- (3) Having deduced estimates of all parasitic resistances associated with the required circuit inductors, the foregoing preliminary computations of inductances, capacitances, and transistor transconductance must now be updated in accordance with the computer-aided optimization guidelines delineated in the preceding subsection of text. The procedure starts by discerning the source terminal inductance, L_{ss} , commensurate with the requisite 50 ohm driving point input impedance at the tuned center frequency of the amplifier. The gate lead inductance, L_{gg} , can then be determined in terms of the revised value of L_{ss} and the originally computed value of the net input circuit inductance, L_{in} . Updated values of the gate-source and gate-drain capacitances, C_{gs} and C_{gd} , respectively, can now be determined in terms of the computed value of net

input capacitance, C_{in} . Armed with the new values of C_{gs} and C_{gd} , as well as with the stipulated value of the transistor unity gain frequency ω_T , the transistor transconductance, g_m , can be updated. Finally, the load circuit inductance commensurate with the desired center frequency gain magnitude of 5 volts/volt can be determined. The small signal model of the subject amplifier can now be simulated to ascertain the propriety of the revised parameter estimates. If necessary, the optimization procedure can be revisited to arrive at an acceptable finalized design result.

In the problem at hand, the optimized circuit parameters are as itemized below. Interestingly enough, the optimized values of inductances, capacitances, and transistor transconductance differ only minimally from their respective, originally computed first order estimates.

$$\begin{aligned}
 R_{ss} &= 0.275 \ \Omega \\
 R_{gg} &= 14.5 \ \Omega \\
 R_l &= 2.75 \ \Omega \\
 Q_o &= 5.278 \\
 k_g &= 1.025 \\
 L_{in} &= 44.02 \text{ nH} \\
 C_{in} &= 158.7 \text{ fF} \\
 L_{ss} &= 184.96 \text{ pH} \\
 L_{gg} &= 44.08 \text{ nH} \\
 L_l &= 1.835 \text{ nH} \\
 C_{gs} &= 156.1 \text{ fF} \\
 C_{gd} &= 3.903 \text{ fF} \\
 g_m &= 42.33 \text{ mmho} \\
 \lambda_b g_m &= 1.267 \text{ mmho}
 \end{aligned}$$

- (4) In order to guarantee that the parasitic capacitances in both the source and drain terminals of the transistor exert negligible influence on the amplifier frequency response, the self-resonant frequencies of both the source and drain inductances should be substantially larger than the tuned center frequency by at least a factor of root ten. Recalling Eqs. (9-174) and (9-209), this restriction means that $C_{ss} \leq 5.134 \text{ pF}$ and $C_l \leq 361.8 \text{ fF}$. Fortunately, the upper limit value of capacitance C_{ss} is far larger than typical bulk-source capacitances. Likewise, the upper bound for capacitance C_l is much larger than representative bulk-drain capacitances. Generally, these device capacitances are of the order of 40% of the gate-source capacitance value. For this design, it is reasonable to presume $C_{ss} = 60 \text{ fF}$ and $C_l = 100 \text{ fF}$, the latter accounting to first order for parasitic capacitance associated with any extrinsic load incident with the amplifier output port.
- (5) The foregoing design computations are effectively summarized by the small signal schematic diagram of the bandpass amplifier offered in Fig. 9.58. The

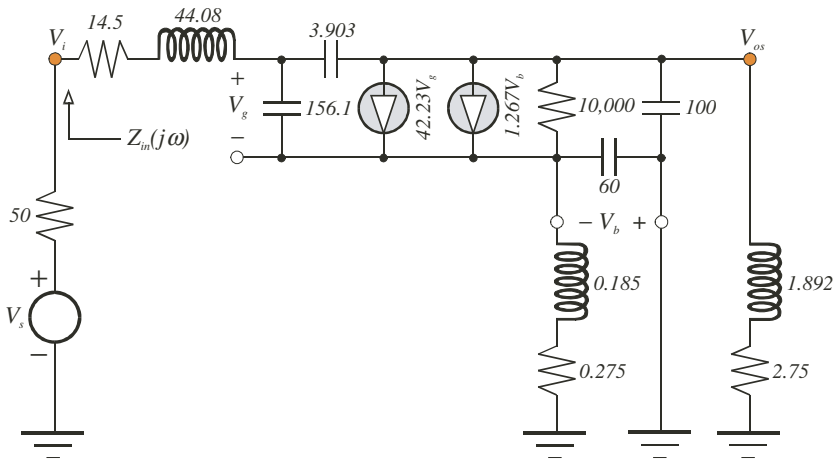


Figure 9.58. Small signal model of the bandpass amplifier designed in Example 9.8. In the diagram, all resistances are in ohms, all inductances are in units of nanohenries, and all capacitances are in femtofarads. Moreover, the conductance multipliers of the two controlled sources are dimensioned in millimhos.

transfer and input impedance characteristics implied by this model were simulated with HSPICE.

Figure 9.59 plots the resistive and reactive components of the driving point input impedance. The reactive portion of this graph is especially interesting, for it serves to pinpoint the resonant frequency of the amplifier. In particular, resonance prevails at the frequency where the reactive input impedance vanishes. A detailed inspection of the simulated data reveals resonance to occur at 1.901 GHz, a scant 0.04% higher than the design target. At 1.901 GHz, the data pertinent to the resistive component of the driving point input impedance offers an input resistance of 50.081 ohms, which is 0.16% above the desired 50 ohm value.

Figure 9.60 displays the overall and input port frequency responses of the amplifier modeled in Fig. 9.58. At the simulated resonant frequency of 1.901 GHz, the data confirms a center frequency *I/O* gain magnitude of 4.98, which is 0.39% below the design target gain magnitude of five. A degradation of this center frequency gain by 3-dB corresponds to an *I/O* gain magnitude of 3.552, which is realized at signal frequencies of 1.737 GHz and 2.093 GHz. The simulated 3-dB bandwidth follows as (2.093 GHz–1.737 GHz), or 356.3 MHz, which is only 1.02% smaller than the design goal of 360 MHz.

The input port frequency response depicted in Fig. 9.60 shows gain magnitudes of nominally unity at both very low and very high frequencies. This result aligns with expectations because the effective series input capacitance, C_{in} ,

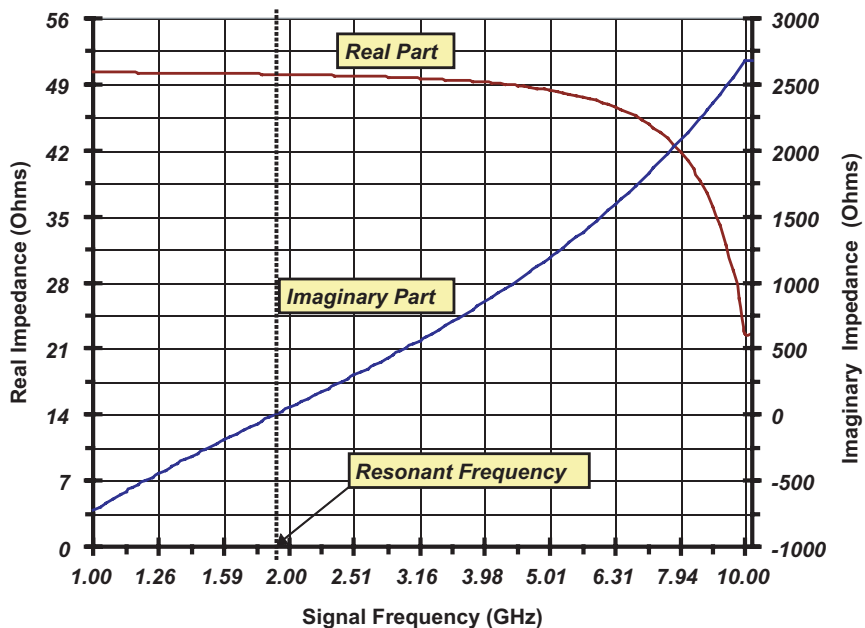


Figure 9.59. Simulated resistive and reactive components of the driving point input impedance, $Z_{in}(j\omega)$, implied by the model in Fig. 9.58.

produces a very large input impedance reactance at low signal frequencies, while the effective series input inductance, L_{in} , likewise yields high reactance at high signal frequencies. At the amplifier center frequency, the input port gain magnitude should be $1/2$ because the amplifier input port is presumably matched to the signal source impedance at the tuned center frequency. A detailed inspection of the simulated data shows that at the simulated center frequency of 1.901 GHz, the I/O gain magnitude is 0.504, which is 0.80% larger than its expected value. This slight discrepancy synergizes with simulated input resistance, which is 0.16% larger than 50 ohms at the center frequency.

Comments. In this example, extraordinarily good agreement is obtained between design predictions of amplifier performance and simulated responses. This good agreement is even more remarkable in light of the fact that the first order design calculations of circuit element values differ only minimally from their optimized counterparts. In order to avoid being lulled into a proverbial false feeling of security, however, it is important to interject that the observed success of this design venture is strongly aided by the fact that the gate-drain capacitance of the utilized transistor is only 1/40th of the transistor gate-source capacitance. Progressively

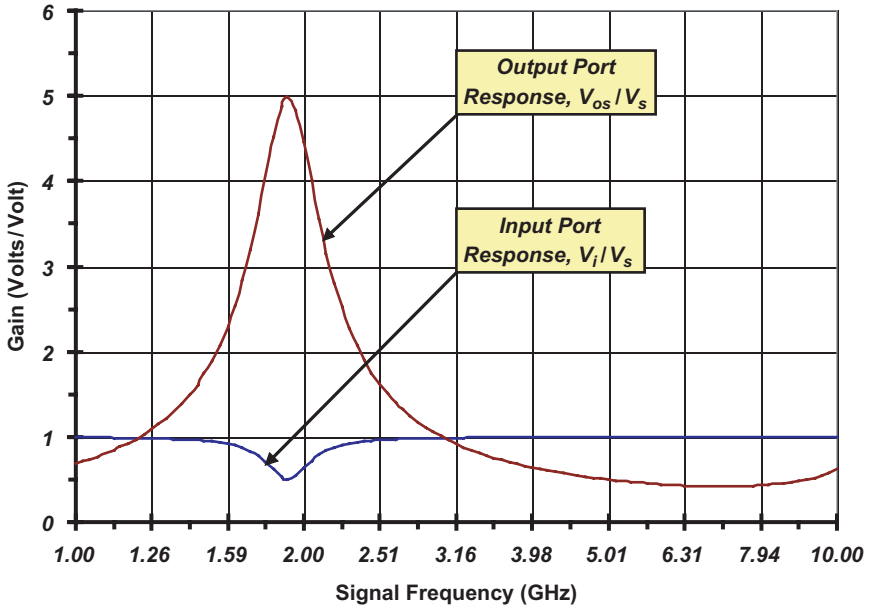


Figure 9.60. Simulated small signal frequency responses of the RF amplifier designed in Example 9.8.

larger gate-drain capacitances can be expected to incur corresponding larger disparities between design objectives and simulated performance. In extreme cases, large gate-drain capacitance may even preclude an acceptable optimization with respect to I/O gain requirements, center frequency goals, and input port impedance matching at the tuned center frequency.

Appreciable gate-drain capacitance causes two, albeit somewhat related, design problems. The first and most obvious of these problems is that the gate-drain capacitance modifies the driving point input impedance by incurring a frequency dependent load on the impedance presented to the input port by the gate to source high frequency current path. Specifically, the latter impedance is $Z_{g_o}(s)$, as incorporated into Eq. (9-180), which also confirms the modification of $Z_{g_o}(s)$ to an impedance, $Z_g(s)$, by a frequency variant factor (the parenthesized term in said equation) that depends on the gate-drain capacitance. The second problem, which is highlighted by this frequency variant factor, is that C_{gd} causes an input port impedance that is perturbed in accordance with a somewhat intricate function of the frequency dependent load termination imposed on the output port of the amplifier. Thus, for example, adjustments made to the drain load inductance, L_l , to achieve a desired center frequency gain are likely to de-tune the input impedance and specifically, the conditions that effect an input port matching to the signal source impedance.

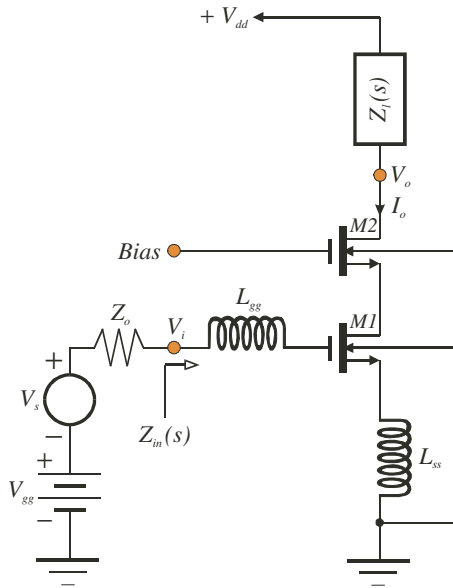


Figure 9.61. The RF amplifier of Fig. 9.53 modified by incorporation of a common gate cascode stage to mitigate the deleterious effects of gate-drain capacitance in the common source driver, $M1$.

The lesson to be learned herewith is that gate-drain capacitance incurs analytical and engineering pain in the design of an inductively degenerated common source RF amplifier. This pain can be treated by inserting a common gate cascode between the drain of the common source amplifier and the inductive load port, as suggested in Fig. 9.61. The principle effect of the cascode transistor, $M2$, is to isolate the inductive load impedance, $Z_l(s)$, from the amplifier input port. If transistors $M1$ and $M2$ have identical geometries, the Miller multiplier of the $M1$ gate-drain capacitance is nominally only a factor of two. To first order, therefore, the gate-source impedance of $M1$ is simply shunted by a capacitance of $2C_{gd}$. Detailed analytical considerations are left as an exercise for the reader.

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Exercises

Problem 9.1

A low frequency gain of at least 20 dB is required of a lowpass amplifier that is to be designed to deliver a 3-dB frequency of 1.0 GHz.

- (a) Determine the optimum number of cascaded identical stages and the corresponding 3-dB bandwidth of each stage if maximum overall bandwidth is to be achieved.
- (b) If the resultant circuit comprises the open loop of a feedback amplifier, plot the magnitude and phase responses of the loop gain for the case

of unity closed loop gain. Comment on the closed loop stability of the amplifier.

Problem 9.2

The approximate transfer function for the compensated amplifier diagrammed in Fig. 9.4(a) is given by Eq. (9-33). Assume that the zero frequency value, $T_s(0)$, of the loop gain is 10.

- Derive an expression for the phase response of the amplifier. Plot this response for $k = 0$, $k = 0.75$, $k = 1$, and $k = 1.25$. Give an engineering assessment of the plotted responses.
- Derive an expression for the transient step response of the amplifier; use an input step amplitude of $1/A(0)$. Plot this response for $k = 0$, $k = 0.75$, $k = 1$, and $k = 1.25$. Give an engineering assessment of the plotted responses. Specifically, discuss the impact exerted on the transient response by the pole-zero doublet.
- Derive an expression for the transient unit impulse response of the amplifier. Plot this response for $k = 0$, $k = 0.75$, $k = 1$, and $k = 1.25$. Give an engineering assessment of the plotted responses.

Problem 9.3

The balanced differential amplifier depicted in Fig. P9.3 is designed for a maximally flat magnitude response and maximal 3-dB bandwidth. All transistors are biased in their saturation domains, all have their bulk terminals connected to their respective source terminals, and all are characterized by infinitely large drain-source channel resistance. Moreover, each transistor features a dominant pole response, with the dominant capacitance established at respective drain terminals.

- Develop a general expression for the differential voltage gain, $A_d(s) = V_o/V_s$.
- Give design criteria that support the objective of a maximally flat, optimally broadbanded, differential frequency response.
- Are common mode input signals a problem in light of the approximations invoked in this exercise?

Problem 9.4

In the cascode configuration of Fig. 9.12, set the inductance, L , to zero and determine all open circuit time constants. Assume that the two transistors are biased in their saturation regimes, have large drain-source channel resistances, and nonmatched small signal parameters. Assuming that pole dominance prevails, deduce the criteria that must be satisfied if the common

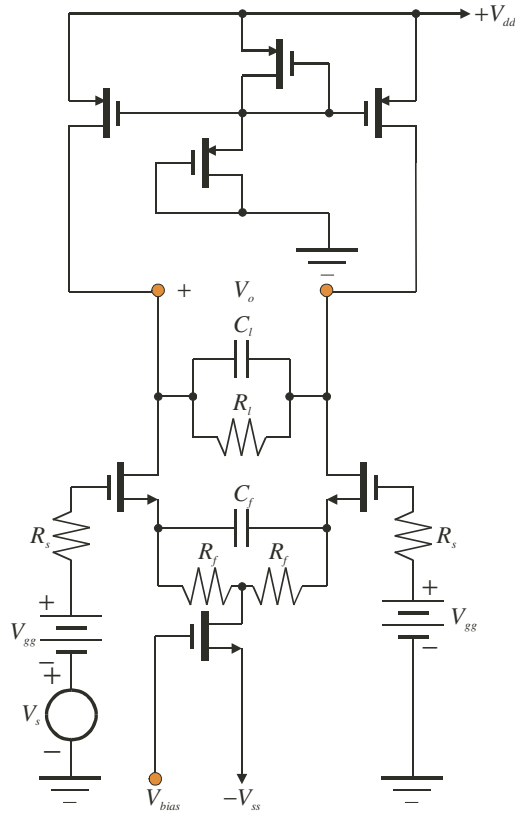


Figure P9.3.

gate cascode is to deliver a 3-dB bandwidth estimate that is larger than that afforded by a conventional common source amplifier.

Problem 9.5

Repeat Example 9.3, but now design for a low frequency voltage gain of 18 dB and a low frequency envelope delay of 200 pSEC. The delay response should emulate, as closely as possible, maximally flat delay. Use the small signal model parameters provided in conjunction with the aforementioned example.

- (a) Provide a finalized small signal model of the completed design realization.

- (b) Use HSPICE or equivalent computer-aided analysis software to simulate the following performance characteristics:
- i. the small signal magnitude response of the amplifier;
 - ii. the small signal phase response of the amplifier;
 - iii. the small signal delay response of the amplifier;
 - iv. the small signal, unit step response of the amplifier.
- (c) Discuss the executed simulations, focusing specifically on any discrepancies observed between theoretically predicted and simulated responses.

Problem 9.6

A third order Bessel filter, which realizes maximally flat delay without benefit of either left half or right half plane zeros has a normalized transfer function of

$$A_n(s) = \frac{1}{1 + (T_{do}s) + \frac{2}{5} (T_{do}s)^2 + \frac{1}{15} (T_{do}s)^3},$$

where T_{do} represents the zero frequency envelope delay between amplifier input and output ports.

- (a) Design a maximally flat delay, series peaked amplifier that supports a voltage gain of 0 dB and a zero frequency delay of 30 pSEC. Use the transistor whose small signal parameters are supplied in conjunction with Example 9.2.
- (b) Use HSPICE or equivalent computer-aided design software to simulate the magnitude response and the envelope delay response.

Problem 9.7

Return to the schematic diagram of the series peaked amplifier shown in Fig. 9.20. Assume that the net capacitance, $(C_o + C_x)$, is negligibly small.

- (a) Derive the condition commensurate with a maximally flat delay (MFD) response.
- (b) What bandwidth enhancement is afforded by selecting inductance L in concert with a maximally flat delay response?
- (c) Derive an expression for the magnitude peaking as a function of circuit quality factor.
- (d) Submit a plot depicting the dependencies of both the magnitude peaking and the 3-dB bandwidth on circuit quality factor.

Problem 9.8

Equation (9-81) defines the approximate voltage transfer function of the series-shunt peaking amplifier of Fig. 9.23 subject to neglect of capacitance C_o and the condition and definition imposed respectively by Eqs. (9-79) and (9-80).

- Derive the bandwidth expression given in Eq. (9-82).
- Show that the frequency at which peaking in the magnitude response is observed is $0.687B_u$, where B_u is the bandwidth of the uncompensated amplifier ($L = 0$) if capacitance C_o is tacitly ignored. Verify that the percentage peaking, measured with respect to the zero frequency value of voltage gain, is just slightly under 3%.

Problem 9.9

Show that from the perspective of the terminal currents, I_1 and I_2 , and the terminal voltages, V_1 and V_2 , the coupled inductor circuit of Fig. P9.9(a) is electrically identical to the structure in Fig. P9.9(b). The parameter, M , signifies the mutual inductance between the two coils of inductance L .

Problem 9.10

Repeat Problem 9.9 for the case in which the two terminals of the inductive coil on the right in Fig. P9.9(a) are interchanged.

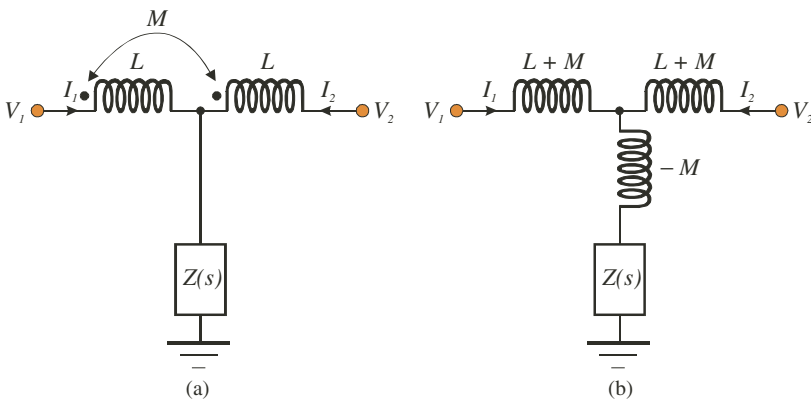


Figure P9.9.

Problem 9.11

Lossless constant resistance networks have been propounded in the technical literature as an effective vehicle for achieving broadband frequency responses in active transconductor amplifiers. One such alternative to the networks addressed in the text is the filter shown in Fig. P9.11, where the terminating load impedance, $Z_o(s)$, is selected to ensure that the driving point input impedance, $Z_{in}(s) \equiv Z_o(s)$. The indicated two inductors are uncoupled.

(a) Show that the required value of load impedance $Z_o(s)$ is expressible as

$$Z_o(s) = R_o \sqrt{1 + \left(\frac{s}{\omega_h}\right)^2}$$

where resistance parameter R_o and frequency parameter ω_h are given by

$$R_o = \sqrt{L/C}$$

and

$$\omega_h = 2/\sqrt{LC}$$

(b) Clearly, a constant driving point input resistance is manifested for a strictly resistive load only for signal frequencies, ω , that satisfy the inequality, $\omega \ll \omega_h$, whereupon, $Z_o(s) \approx R_o$. For this resistive load constraint, demonstrate that the voltage transfer function, $H_o(s) = V_o/V_s$, mirrors that of a Butterworth filter.

(c) What is the 3-dB bandwidth associated with the transfer function, $H_o(s)$, deduced in Part (b)?

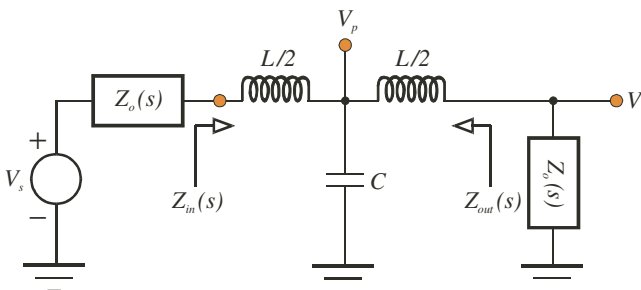


Figure P9.11.

- (d) For $Z_o(s) = R_o$, derive an expression for the transfer function, $H_p(s) = V_p/V_s$. Is this transfer characteristic representative of a Butterworth filter?
- (e) What is the zero frequency group delay associated with the transfer function, $H_o(s)$?

Problem 9.12

Yet another lossless, constant resistance structure is shown in Fig. P9.12, where the terminating load impedance, $Z_o(s)$, is to be selected to ensure that the driving point input impedance, $Z_{in}(s) \equiv Z_o(s)$.

- (a) Show that the required value of load impedance $Z_o(s)$ is expressible as

$$Z_o(s) = \frac{R_o}{\sqrt{1 + \left(\frac{s}{\omega_h}\right)^2}},$$

where

$$R_o = \sqrt{L/C}$$

and

$$\omega_h = 2/\sqrt{LC}.$$

- (b) Clearly, a constant driving point input resistance is manifested for a strictly resistive load only for signal frequencies, ω , that satisfy the inequality, $\omega \ll \omega_h$, whereupon, $Z_o(s) \approx R_o$. For this resistive load constraint, demonstrate that the voltage transfer function, $H_o(s) = V_o/V_s$, mirrors that of a Butterworth filter.

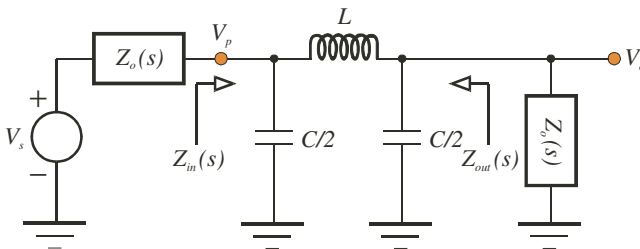


Figure P9.12.

- (c) What is the 3-dB bandwidth associated with the transfer function, $H_o(s)$, deduced in Part (b)?
- (d) For $Z_o(s) = R_o$, derive an expression for the transfer function, $H_p(s) = V_p/V_s$. Is this transfer characteristic representative of a Butterworth filter?
- (e) What is the zero frequency group delay associated with the transfer function, $H_o(s)$?

Problem 9.13

For the amplifier modeled in Fig. 9.27(b), what inductor coupling coefficient yields a maximally flat group delay response for the transfer function, V_{os}/V_s ? What 3-dB bandwidth is manifested by this maximally flat delay constraint?

Problem 9.14

Repeat all parts of Example 9.5 but this time, design for a maximally flat group delay response that delivers a zero frequency group delay of 20 pSEC.

Problem 9.15

An f_T -doubler can be realized straightforwardly as a balanced differential pair, as suggested by the simplified schematic diagram in Fig. P9.15 in which both transistors are identical devices that are biased identically.

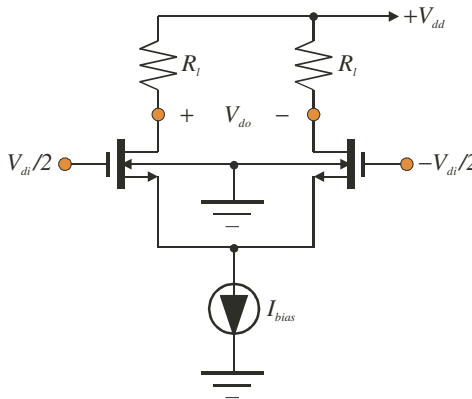


Figure P9.15.

- (a) Give an engineering argument that rationalizes the presumed doubling of the unity gain frequency of each transistor when the circuit is operated as a differential amplifier.
- (b) Execute a small signal analysis of the circuit to confirm the presumed doubling of transistor f_T .
- (c) Does this problem teach the advisability of realizing all amplifiers designed for broadbanded frequency responses as balanced differential pairs? What engineering circumstances must prevail if differential circuit technology is to prove effective as a broadband topological tool?

Problem 9.16

Repeat Example 9.6 in the text for the case in which the gate-drain capacitance is 5% of the transistor gate-source capacitance, and the desired gain is 20 dB.

Problem 9.17

Repeat Example 9.7 in the text for case in which input port matching is implemented.

Problem 9.18

Generate a curve, similar to that supplied in the text as Fig. 9.49, for the case in which transistors exuding a 45 GHz unity gain frequency are exploited in the f_T -doubler of Fig. 9.47.

Problem 9.19

Repeat Example 9.6, but let the transistor embedded in the dual loop feedback amplifier shown in Fig. 9.32 be replaced by the f_T -doubler configuration offered in Fig. 9.47. Assume that the transistors in the doubler have a unity gain frequency of 28 GHz.

Problem 9.20

Perform a small signal analysis of the short circuit current gain response of the Battjes f_T -doubler, whose basic circuit schematic diagram appears in Fig. 9.50. Assume that the transistors utilized in the Battjes circuit have negligible gate-drain capacitance, are geometrically identical, and are biased identically.

Problem 9.21

In the cascode RF amplifier of Fig. 9.61, assume identical transistors that are biased identically and that are characterized by very large drain-source

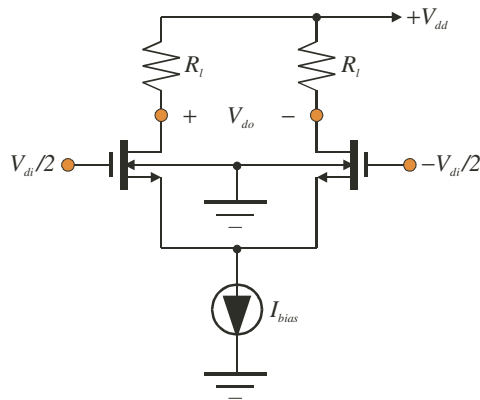


Figure 9.21.

channel resistances and negligibly small bulk-induced threshold voltage modulation factors. Assume further that the source terminal inductance, L_{ss} , as well as the drain load impedance, $Z_l(s)$, are realized as monolithic inductances. Analyze the circuit in a fashion similar to the work executed in Section 9.9.2 of the text so that appropriate responses can be generated to the following inquiries.

- Give an expression for the net effective series input resistance, R_{in} .
- Derive an expression for the net effective input port inductance, L_{in} .
- Derive an expression for the net effective input port capacitance, C_{in} .
- Deduce a relationship for the tuned center frequency, ω_o , of the RF amplifier.
- Deduce an expression for the 3-dB bandwidth of the amplifier.
- How must inductance L_{ss} be chosen to achieve an input port impedance match to a resistive source impedance at the tuned center frequency of the amplifier?
- Assuming input port matching, what is the amplifier voltage gain, H_o , at the tuned center frequency?
- What is the time constant established at the source terminal of transistor $M2$? What condition must be satisfied by this time constant if proper amplifier operation is to be ensured?
- What is the net capacitance that prevails at the amplifier output port? What condition must be satisfied by this capacitance if proper amplifier operation is to be ensured?

Problem 9.22

Using the results of the preceding exercise, repeat Example 9.8, but use the cascode configuration offered in Fig. 9.61. Comment as to the overall engineering quality of this amplifier, as compared to the amplifier specifically addressed in Example 9.8.

Problem 9.23

The transistor used in the source follower depicted in Fig. P9.23 is biased in its saturation regime. For the purposes of this problem, assume that the transistor is characterized by an infinitely large drain-source channel resistance and a negligibly small bulk-induced threshold modulation factor. Observe that the follower drives a capacitive load of capacitance C_l , and since the circuit is intended for use in high frequency signal processing applications, the gate-source, bulk-source, bulk-drain, and gate-drain capacitances of the device cannot be ignored.

- Derive an expression for the small signal, driving point input impedance, $Z_{in}(s)$.
- In the sinusoidal steady state, what is the reactive component of the driving point input impedance found in Part (a)? Is the input port of the follower capacitive or inductive at high signal frequencies?
- In the sinusoidal steady state, what is the real part component of the driving point input impedance found in Part (a)? Determine the load capacitance conditions that deliver a negative real input impedance.
- What are the engineering implications, with respect to the transient pulse response of a source follower, of a negative real part input impedance?

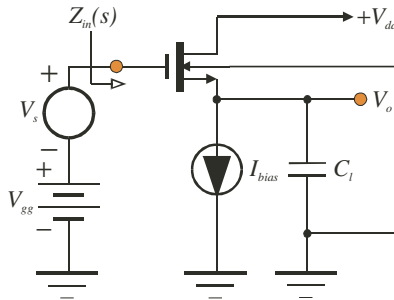


Figure P9.23.

- (e) Compensate the circuit to alleviate the high frequency negative resistance problem to which the preceding part of this problem alludes. Provide design guidelines or formulae for any compensation elements added to the circuit.

Problem 9.24

The transistor used in the source follower depicted in Fig. P9.24 is biased in its saturation regime. For the purposes of this problem, assume that the transistor is characterized by an infinitely large drain-source channel resistance and a negligibly small bulk-induced threshold modulation factor. Observe that the follower drives an inductive load of inductance, L_l , and since the circuit is intended for use in high frequency signal processing applications, the gate-source, bulk-source, bulk-drain, and gate-drain capacitances of the device cannot be ignored. The load inductance is realized monolithically, so that an account of series resistance and shunt parasitic capacitance must be made.

- (a) Derive an expression for the small signal, driving point input impedance, $Z_{in}(s)$.
- (b) In the sinusoidal steady state, what is the reactive component of the driving point input impedance found in Part (a)? Is the input port of the follower capacitive or inductive at high signal frequencies?
- (c) In the sinusoidal steady state, what is the real part component of the driving point input impedance found in Part (a)? Determine the load inductance conditions that deliver a negative real input impedance.
- (d) Compensate the circuit to alleviate any high frequency negative resistance problems to which the preceding part of this problem alludes. Provide design guidelines or formulae for any compensation elements added to the circuit.

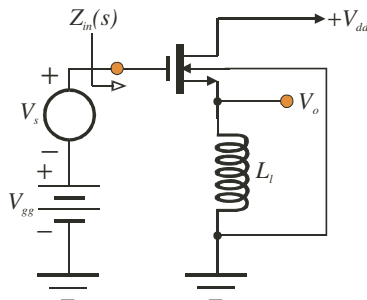


Figure P9.24.

Problem 9.25

A common gate circuit used as a cascode in conjunction with a common source amplifier engenders potential engineering design problems because of parasitic layout inductance manifested in the gate lead of the circuit. To this end, consider the circuit shown in Fig. P9.25, in which the transistor is characterized by an infinitely large drain-source channel resistance and a negligibly small bulk-induced threshold modulation factor. All relevant device capacitances should not be ignored so that due account can be made of relevant high frequency phenomena. The inductance, L_g , in the gate lead can be presumed to be an ideal element.

- (a) Derive an expression for the indicated small signal, source input impedance, $Z_{in}(s)$.
- (b) In the sinusoidal steady state, what is the reactive component of the source input impedance found in Part (a)? Is the input port of the common gate stage capacitive or inductive at high signal frequencies?
- (c) In the sinusoidal steady state, what is the real part component of the driving point impedance found in Part (a)? Determine the gate inductance conditions that deliver a negative real source input impedance.
- (d) Compensate the circuit to alleviate any high frequency negative resistance problems to which the preceding part of this problem alludes. Provide design guidelines or formulae for any compensation elements added to the circuit.

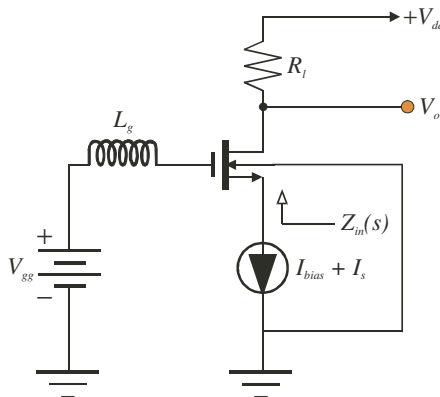


Figure P9.25.