

Contents

Foreword	vii
Preface	ix
Chapter 1 Introduction	1
1.1 VLSI Design	1
1.2 The VLSI Design Process	2
1.2.1 Architectural Design	3
1.2.2 Logic Design	7
1.2.3 Physical Design	7
1.3 Layout Styles	9
1.3.1 Full-custom Layout	9
1.3.2 Gate-array Layout	12
1.3.3 Standard-cell Layout	14
1.3.4 Macro-cell Layout	17
1.3.5 Programmable Logic Arrays	19
1.3.6 FPGA layout	21
1.4 Difficulties in Physical Design	23
1.4.1 Problem Subdivision	24
1.4.2 Computational Complexity of Layout Subproblems	25
1.4.3 Solution Quality	27
1.5 Definitions and Notation	27
1.5.1 Nets and Netlists	28
1.5.2 Connectivity Information	29
1.5.3 Weighted Nets	32
1.5.4 Grids, Trees, and Distances	32

1.6	Summary	34
1.7	Organization of the book	36
Chapter 2 Circuit Partitioning		41
2.1	Introduction	41
2.2	Problem Definition	43
2.3	Cost Function and Constraints	44
	2.3.1 Bounded Size Partitions	44
	2.3.2 Minimize External Wiring	45
2.4	Approaches to Partitioning Problem	46
	2.4.1 Kernighan-Lin Algorithm	48
	2.4.2 Variations of Kernighan-Lin Algorithm	58
	2.4.3 Fiduccia Mattheyses Heuristic	59
	2.4.4 Simulated Annealing	70
2.5	Other Approaches and Recent Work	80
2.6	Conclusion	82
2.7	Bibliographic Notes	83
Chapter 3 Floorplanning		91
3.1	Introduction	91
3.2	Problem Definition	92
	3.2.1 Floorplanning Model	92
	3.2.2 Cost Functions	94
	3.2.3 Terminology	96
3.3	Approaches to Floorplanning	101
	3.3.1 Cluster Growth	102
	3.3.2 Simulated Annealing	108
	3.3.3 Analytical Technique	122
	3.3.4 Dual Graph Technique	130
3.4	Other Approaches and Recent Work	149
3.5	Conclusion	151
3.6	Bibliographic Notes	152
Chapter 4 Placement		161
4.1	Introduction	161
	4.1.1 Complexity of Placement	163
	4.1.2 Organization of the Chapter	164
4.2	Problem Definition	164
4.3	Cost Functions and Constraints	165

4.3.1	Estimation of Wirelength	165
4.3.2	Minimize Total Wirelength	168
4.3.3	Minimize Maximum Cut	169
4.3.4	Minimize Maximum Density	172
4.3.5	Maximize Performance	173
4.3.6	Other Constraints	175
4.4	Approaches to Placement	176
4.4.1	Partition-Based Methods	179
4.4.2	Limitation of the Min-cut Heuristic	184
4.4.3	Simulated Annealing	189
4.4.4	Numerical Techniques	197
4.5	Other Approaches and Recent Work	206
4.5.1	Artificial Neural Networks	206
4.5.2	Genetic Algorithm	211
4.6	Conclusion	219
4.7	Bibliographic Notes	220
Chapter 5 Grid Routing		233
5.1	Introduction	233
5.2	Problem Definition	234
5.3	Cost Functions and Constraints	235
5.3.1	Placement Constraints	237
5.3.2	Number of Routing Layers	237
5.3.3	Geometrical Constraints	238
5.4	Maze Routing Algorithms	238
5.4.1	Lee Algorithm	239
5.4.2	Limitations of Lee Algorithm for Large Circuits	241
5.4.3	Connecting Multi-point Nets	244
5.4.4	Finding More Desirable Paths	246
5.4.5	Further Speed Improvements	250
5.5	Line Search Algorithms	253
5.6	Other Issues	256
5.6.1	Multi Layer Routing	257
5.6.2	Ordering of Nets	260
5.6.3	Rip-up and Rerouting	265
5.6.4	Power and Ground Routing	265
5.7	Other Approaches and Recent Work	267
5.8	Conclusions	268

5.9	Bibliographic Notes	269
Chapter 6 Global Routing		277
6.1	Introduction	277
6.2	Cost Functions and Constraints	278
6.3	Routing Regions	279
6.3.1	Routing Regions Definition	280
6.3.2	Routing Regions Representation	290
6.4	Sequential Global Routing	292
6.4.1	The Steiner Tree Problem	293
6.4.2	Global Routing by Maze Running	296
6.5	Integer Programming	302
6.6	Global Routing by Simulated Annealing	306
6.6.1	The First Stage	307
6.6.2	The Second Stage	312
6.7	Hierarchical Global Routing	313
6.8	Other Approaches and Recent Work	315
6.9	Conclusions	318
6.10	Bibliographic Notes	319
Chapter 7 Channel Routing		327
7.1	Introduction	327
7.2	Problem Definition	328
7.2.1	Constraint Graphs	329
7.3	Cost function and Constraints	332
7.4	Approaches to Channel Routing	333
7.4.1	The Basic Left-Edge Algorithm	333
7.4.2	Dogleg Algorithm	338
7.4.3	Yoshimura and Kuh Algorithm	341
7.4.4	Greedy Channel Router	352
7.4.5	Switchbox Routing	359
7.5	Other Approaches and Recent Work	364
7.6	Conclusions	372
7.7	Bibliographic Notes	373
Chapter 8 Layout Generation		377
8.1	Introduction	377
8.1.1	Behavioral Level	377
8.1.2	Structural Level	378

8.1.3	Physical Level	379
8.2	Layout Generation	383
8.2.1	Standard-cells	385
8.2.2	Gate-matrix Methodology	386
8.2.3	Programmable Logic Array	386
8.3	Standard-cell Generation	388
8.3.1	Optimization of Standard-cell Layout	391
8.4	Optimization of Gate-matrix Layout	397
8.5	Programmable Logic Arrays	405
8.5.1	PLA Personality	408
8.5.2	Optimization of PLAs	410
8.6	Other Approaches and Recent Work	422
8.7	Conclusion	426
8.8	Bibliographic Notes	426
Chapter 9 Layout Editors and Compaction		433
9.1	Introduction	433
9.1.1	Capabilities of Layout Editors	434
9.1.2	Introduction to Magic Layout System	435
9.2	Layout Compaction	441
9.2.1	Compaction Algorithms	444
9.2.2	Horizontal Virtual Grid Compaction	445
9.2.3	Constraint Graph Compaction	447
9.3	Other Approaches and Recent Work	454
9.4	Conclusion	455
9.5	Bibliographic Notes	456
Appendix A Graph Theory and Complexity of Algorithms		463
A.1	Graph Theory	463
A.2	Complexity of Algorithms	465
A.2.1	Big-Omega Notation	466
A.2.2	Big-Oh Notation	466
A.2.3	Big-Theta Notation	467
A.3	Hard Problems vs. Easy Problems	467
A.3.1	NP-complete Problems and Reduction	469
Index		471