

Overview 1

Even though the operation of the modern **Metal-Oxide-Semiconductor** (MOS) transistor was first described by Lilienfield in 1930 [1], it was not until 1960 that the first MOS transistor using silicon as the semiconductor material was reported by Kang and Atalla [2]. The MOS technology became viable only after methods of routinely growing reliable oxides were developed and reported by Snow, Grove, Deal and Sah in 1964 [3]. Since that time the MOS industry has expanded very quickly. Today MOS integrated circuits (ICs) have emerged as the dominant technology in the semiconductor industry. The exponential growth in the number of components per chip and projections for the future are shown in Figure 1.1 [4]. Also shown is the minimum feature size that can be produced on a chip. The dotted lines are projections for the future. Clearly with this technology it is now possible to have more than a million transistors on a single chip. All this has been possible due to the fact that the basic MOS transistor size has shrunk by a factor of about 20 during the last two decades, from a feature size of $20\ \mu\text{m}$ to less than a micron. Much of this shrinkage can be attributed to advances in lithography, the use of ion implantation, and low temperature annealing [4].

During the early days of MOS technology, aluminum (Al) gate *p*-channel MOS transistors were the workhorse technology. In the late sixties polysilicon replaced Al as the material for the MOS transistor gate [5]. The next major milestone was the LOCOS (LOCALized Oxidation of Silicon) isolation technique [6]. Commercially successful products using the NMOS process (all *n*-channel MOS transistors) with LOCOS isolation were developed in the mid seventies. NMOS device technology became the driving force of the 1970s because of its reliability, reasonable manufacturing cost, and scalability. During the last decade, MOS transistors have been scaled down in dimensions both vertically and horizontally. Rules of this scaling were originally formulated by Dennard et al. [7] in 1974 and subsequently other schemes of scaling were proposed [8] (see Section 3.3).

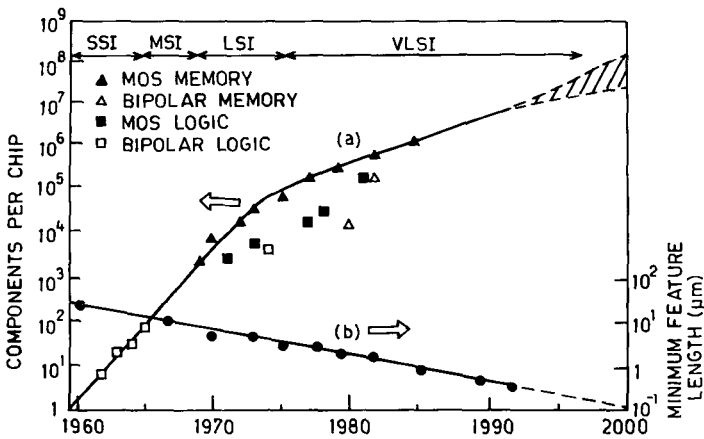


Fig. 1.1 (a) Exponential growth of the number of components on the chip (SSI = small-scale integration; MSI = medium-scale integration; LSI = large-scale integration; VLSI = very large-scale integration); (b) Exponential decrease of the minimum device dimensions. Dotted lines are projections. (From Sze [4, p. 3], slightly modified)

Unfortunately not all device parameters can be scaled proportionately. *These limits on scaling have increased the importance of device and circuit modeling.* The CMOS (Complementary MOS, with both p - and n -channel transistors) technology has revolutionized the state of the art of IC design due to its inherent noise immunity and reduced static power dissipation. CMOS technology became the technology of choice for the VLSI (Very Large Scale Integration) chips of the 1980s [9]. Although there has been considerable recent interest in incorporating bipolar transistors into CMOS processes, resulting in a BiCMOS technology [10, 11], we will restrict ourselves to device modeling for NMOS and CMOS technologies.

Although the MOS transistor (also called MOSFET) is the most important device for VLSI chips such as microprocessors and semiconductor memories, it is also becoming an important power device. MOS transistors based on DMOS (Double-diffused MOS) and VMOS (Vertical grooved MOS) technology have highly asymmetrical characteristics which makes these technologies unsuitable for integrated circuit applications [12]. Nevertheless, excellent discrete power devices are built with these technologies. The modeling of power MOSFETs is not covered in this book [13, 14].

1.1 Circuit Design with MOSFETs

For today's circuit design, computer-aided simulation [15]–[17] has become an indispensable tool because:

- Manual techniques traditionally used for circuit analysis and design are simply inadequate because of the complexity of today's circuits.
- Simulation allows designers to design their chips under worst case conditions so that manufacturing tolerances can be incorporated into the design. It thus greatly increases the likelihood that the circuit (chip) will work as desired and have good production yield.
- Simulation allows designers to predict and optimize circuit performance.

At the lower end of the hierarchy of VLSI design tools, *circuit simulators* offer the most detailed level of simulation normally used for circuit design. Some of the most successful circuit simulators of the early 1970s are still used extensively in the design and verification of VLSI chips; most notably are ASTAP(Advanced STatistical Analysis Program) from IBM [18] and SPICE2(Simulation Program with Integrated Circuit Emphasis) from the University of California, Berkeley¹ [19]. These simulators are typically used to analyze circuits with up to several hundred nodes. SPICE2 is the defacto industry standard and is used in many universities all over the world. Most of the circuit simulators which are available commercially are derived from SPICE. The commercial vendors claim to provide improved convergence, graphics capabilities, improved user interfaces, and often special analysis modes. Simulators that are not derived from SPICE differ from it in their choice of integration methods or in some aspect of modeling methodology. A very good survey of different commercially available circuit simulators was reported by Beresford and Domitrowich [20]. The capabilities of these simulators includes three basic types of analysis, e.g. nonlinear DC, nonlinear transient and linear AC analysis and several special options such as sensitivity analysis, noise and distortion analysis, worst case analysis, and Fourier analysis. In recent years relaxation based circuit simulators for special classes of MOS circuits have emerged that could speedup the simulation of big circuits by at least two orders of magnitude [21].

In general a circuit simulation program consists of the following four subprograms [22]–[24]: (1) the *input* subprogram that reads the input file, constructs the data structure for the original circuit description and checks

¹ SPICE3 is a redesigned implementation of SPICE2 program written in the C programming language and is designed to be modular. In terms of algorithms it is no improvement over SPICE2 which is written in Fortran. The SPICE software package is in public domain and can be obtained by writing to Ms. Cindy Manly, EECS/ERL Industrial Liaison Program, 497 Cory Hall, University of California, Berkeley, California, 94720.

it for user errors; (2) the *setup* subprogram that sets up data structures required for the circuit analysis; (3) the *analysis* subprogram which performs the desired circuit analysis; and (4) the *output* subprogram which generates the output specified by the user. It is the analysis part where the system of equations describing the complete circuit are solved numerically to give the desired analysis results. This system of equations is formed for each element in the circuit and the topological constraint connecting them. In general, it is of the form

$$\mathbf{f}(\mathbf{x}, \mathbf{x}', t) = 0 \quad (1.1)$$

where \mathbf{x} is the vector of the unknown circuit variables, \mathbf{x}' is the time derivative of \mathbf{x} , t is the time, and \mathbf{f} in general is a highly nonlinear function vector. A solution of Eq. (1.1) can be obtained by first converting nonlinear differential equations into nonlinear algebraic equations using numerical integration methods. The resulting nonlinear algebraic equations are then solved using the Newton–Raphson iterative algorithm. At each Newton–Raphson iteration the nonlinear equations are linearized around the operating point. The linear representation of nonlinear circuit elements like diodes and transistors is called the *companion model*. The latter describes the linearized characteristics of the nonlinear element as a function of its controlling voltage and current. The differential equation characterizing a capacitor or inductor is also approximated using a companion model (resistive circuit) that depends upon the integration algorithm [22, 23]. Thus a *companion model reduces a dynamic network into a resistive network*. It should be pointed out that the linearization process is approximate and therefore its accuracy depends on the error tolerance allowed.

Numerical errors are unavoidable in the simulation process. However, by choosing suitable variables these errors may be reduced. From the computational point of view, when the circuit contains nonlinear capacitors it is advantageous to use charge Q as the state variable as this has been shown to result in less propagation of numerical error [22]. For MOSFET capacitances this choice of Q as a state variable becomes essential. Otherwise charge nonconservation problems can arise, as will be discussed in detail in Chapter 7.

The utility of the circuit simulators as a tool for the design and analysis of VLSI circuits depends on the adequacy of the device model being used in the simulator. In particular, the accuracy and simplicity (computational efficiency) of the model directly affects the corresponding accuracy and speed of simulation. It has been found that for large circuits the MOSFET model evaluation accounts for a large percentage (up to 80%) of the total analysis time [15]. This problem is further aggravated by the technology trend towards smaller and smaller device dimensions which increases the complexities of the models. Thus realistic circuit modeling requires an understanding of the accuracy and limitations of the various device models

and the computational techniques used for performing the analysis of the model.

1.2 MOSFET Modeling

The device models describe the terminal behavior of a device in terms of current-voltage (I-V), capacitance-voltage (C-V) characteristics, and the carrier transport process which takes place within the device. These models thus reflect device behavior in all regions of operation of the device. It is convenient to divide these models into two categories: (1) physical device models, and (2) equivalent circuit models. Physical device models are based on a careful definition of device geometry, doping profile, carrier transport equations (*semiconductor equations*) and material characteristics. These models can be used to predict both terminal characteristics and transport phenomenon. Modern MOS VLSI devices, due to their small size (micron and submicron), require two- or three-dimensional solutions of the coupled semiconductor equations which can be solved only by numerical methods [25,26]. These so called numerical *device simulators* provide detailed insight into the physical aspect of device operation and can predict the characteristics of new devices. For this reason they are mostly used to study device physics and device design [27]. Several public domain and commercial software packages are now available for device analysis and simulation; the most well known among them are MINIMOS [28], PISCES [29], FIELDAY [30], CADDETH [31]. Since device simulators are computationally intensive and require large amount of computer memory, they are not suitable for circuit simulation.

Due to the 2-D and 3-D nature of the physical effects governing electrical behavior of VLSI MOS transistors, it is very difficult to obtain a closed form analytical formulation which is valid in all operating regions of interest. However, *one can still obtain closed form analytical models, based on device physics, that are generally valid only over a limited region of device operation.* Despite this limitation, such models are frequently used for circuit simulators because of ease of computation.

Equivalent circuit models describe electrical properties of the device by connecting electrical circuit elements in such a way that the model emulates the electrical terminal behavior of the device. These models are thus based on the device characteristics; the circuit elements of this model are derived either from closed form analytical function or using an empirical approach. These models are often used in circuit simulators to represent device characteristics because of the ease of evaluation; the circuit simulator SPICE exclusively uses equivalent circuit models. For semiconductor devices the equivalent circuit model elements are highly nonlinear and element values are strongly dependent on DC bias, frequency, signal level and temperature.

Therefore, in addition to having separate DC and AC circuit models, it is generally necessary to distinguish between the small-signal and large-signal (transient) models. Thus in general we require three types of circuit models—DC, transient and AC—corresponding to three basic types of circuit analysis:

- A DC model is a *static model* that evaluates the device current for a fixed voltage, not varying with time. Thus in a DC model dynamic effects such as time delay arising from the presence of energy-storage elements (capacitors and inductors) are ignored. This model is used to calculate quiescent operating points of a circuit.²
- A transient model is a *large-signal dynamic model* which evaluates the device current when the applied voltage is varying with time. It is called a large-signal model because no restrictions are placed on the magnitude of the applied voltage. This model is required for the time domain analysis. In this case current is the sum of both DC and transient currents arising from the charging or discharging of device storage elements, usually capacitances.
- An AC model is a *small-signal model* which evaluates the current when the variation in the applied voltage is so small that the resulting small current variations can be expressed using linear relations. The small-signal linear model can usually be obtained very easily and systematically from the DC model of the device. Since AC model is used for the frequency-domain analysis, it should take into account energy-storage elements and the frequency dependent effects of the transistor.

The MOSFET model we will be concerned with contains only capacitances as the storage elements and not the inductors. The latter are important only at very high frequencies (GHz range). For the transistor model to be used in a circuit simulator, the following requirements should be satisfied:

- The model should be *accurate* so that it simulates actual transistor behavior over all regions of operation of interest. An accuracy of about 5% between the experimental device current (and capacitances) and the model is generally sufficient for circuit modeling work.
- During transient analysis, calculation of transistor current is carried out thousands of times, therefore, it is imperative that the model be both *computationally efficient*, and accurate. Thus, the model needs not only to be accurate but *simple* too; there is always a trade-off between accuracy and simplicity.
- In order to avoid any nonconvergence problems in the simulator, the

² The points (nodal voltages and branch currents) about which the circuit operates are termed *quiescent points* (Q-points) or *bias points*. Accurate Q-points are critical for the design and simulation of transient and AC response.

mathematical equations representing the device model must be continuous, with continuous first derivatives (which are required by the Newton–Raphson algorithm), although not necessarily in a strict mathematical sense. The degree of discontinuity, if present, must be so small that the resulting errors can be absorbed by the overall simulation program error tolerances.

- In MOS VLSI circuit design devices of different lengths and widths are used, therefore, it is desirable that a single model should fit all device sizes used in actual design practice.

Clearly, any choice of the model must be based on compromises between the accuracy of the model in predicting device characteristics over the operating range of interest and the computational efficiency of simulating large circuits. As the size and the complexity of modern circuits increases, the choice of appropriate models becomes more critical. For this reason a hierarchy of models of different levels of accuracy are normally available in a circuit simulator so that designers can choose a model best suited to their potential application. For example, Berkeley SPICE has four different levels of MOSFET models. The combined requirements of computational efficiency and available memory restrict the device models for circuit simulators into the following three categories.

Analytical Models. There are basically two types of analytical models where model equations are directly derived from device physics. One type of model is based on surface potential analysis, often called *charge sheet models* [32, 33]. These models are inherently continuous in all regions of operation of the device. The current can be accurately determined using these models, but the equations themselves are complex, involving transcendental expressions, and often require iterations just to compute the surface potential for a given bias condition. They are thus not very suitable for VLSI circuit simulation, although recently they have been used for simulation of small circuits [34, 35]. The second type of analytical model is the result of applying various approximations to the semiconductor equations, based upon decisions as to which physical phenomena dominate [8], [33], [36]–[38]. Thus, different equations are required to represent different regions of operation of the device. Such models represent first order device behavior fairly accurately, and higher order effects are normally accounted for through the introduction of physical and empirical parameters. These models are usually referred to as *semi-empirical analytical models*. *Practically all the models used in today's circuit simulators fall into this category, and range from simple to more complex models.* These are the type of models which are covered in this book.

The advantage of these models are that they do describe the relationship between the physical process and geometry structure on the one hand and

electrical behavior on the other, so that with some minor changes in the process, electrical behavior can still be predicted. However, the disadvantage is that they are technology dependent and takes considerable time to develop the model. Furthermore, effects resulting from new device structures often require minor or major modification of the existing model and may even require a new model.

Table Lookup Model. In a table lookup model the device current data are stored for different bias points and device geometries in a tabular form [39]–[41]. Generally some sort of interpolation scheme is used to obtain the current values which are not stored. This data base is collected from experimental devices or generated from device level simulators like MINIMOS/PISCES. In another approach, instead of directly storing the device current I_{ds} , the coefficient of some mathematical functions like cubic splines are precalculated from original I_{ds} data for different bias and geometry. It is the coefficients of this function which are then stored in a tabular form, and are later used to compute the currents and conductances required by the simulator [40]–[41]. This approach increases model evaluation speed and reduces storage. *These types of models have the advantage that they are technology independent and can be developed in a shorter time compared to physical models.* The disadvantage of this approach is that it gives no physical insight into device behavior. The model validity outside the data range is uncertain, and if accuracy is required storage is still a problem.

It should be pointed out that table lookup models are generally used for device DC models. For transient and AC models, we still use analytical models because the charges associated with different device terminals are difficult to measure. The charges can be calculated from terminal capacitances [42], but even the capacitance measurements for VLSI devices are difficult to carryout. We will not cover the table lookup model and the interested reader should look into the references cited.

Empirical Model. In an empirical model, the model equations representing device characteristics are purely of the curve fitting type and are thus not based on device physics [42a]. The only advantage of this type of model is that it requires small data storage as compared to table look models and model development time is shorter compared to other modeling approaches. The disadvantage is that this approach is not technology independent. *Purely empirical models are seldom used in circuit simulators,* although empirical (or curve fitting) parameters are often included in physical models to describe 2 or 3-D device behavior.

1.3 Model Parameter Determination

The accuracy of a device model in predicting device characteristics is fully dependent on the accuracy of the model parameter values being used. With ever decreasing device dimensions, the complexity of the models used in circuit simulators have increased significantly. Further, most circuit models are semi-empirical analytical models containing various fitting parameters that do not have a well defined physical meaning, and the number of these fitting parameters increases with the complexity of the model. Very often some of these fitting parameters become redundant,³ and no unique value can be determined for those parameters. Therefore, care must be taken in extracting model parameter values from device data so that physical meaning of the parameter is retained as far as possible. The device data required for extracting model parameters may either be obtained from a device level simulator or from electrical measurements on a number of test devices of different geometries (different widths and lengths). For MOS VLSI it is common practice to fabricate MOS transistors of different widths and lengths on special test chips, also called *test patterns*, along with other test structures required for process development and characterization [43]. The electrical measurements on test transistors are then normally performed using an automatic wafer prober and measurement system as discussed in Chapter 9.

Various general purpose curve fitting programs called *optimizers* have been developed which extract model parameters by curve fitting model equations to the experimental device data using non-linear least square optimization techniques [44]–[46]. One such optimizer which is in the public domain is SUXES (Stanford University eXtractor modEl parameterS) from Stanford University.⁴ Other similar packages are commercially available from different companies and universities.

To support designs that yield well across the full range of random variations in a process, the statistical behavior of the model parameters must be known. Since I-V and/or C-V characteristics of the devices represent the joint distribution of all the process variations, by extracting the model parameters from these curves for different size MOSFETs, and studying the observed distribution of extracted parameters, worst case design parameters can be created. This process spread information is essential for chip design for good manufacturing yield (see Chapter 12).

³ If a physical effect can be described partially by two parameters or one parameter has much smaller influence than the other parameter, then one of the parameter becomes redundant.

⁴ SUXES can be obtained by writing to Office of Technical Licensing, Stanford University, 105 Encina Hall, Stanford, California 94305.

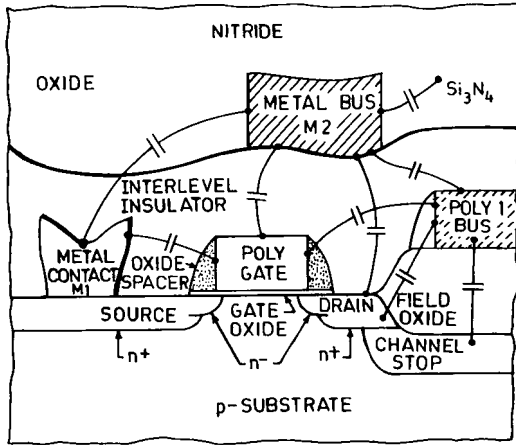


Fig. 1.2 Parasitic capacitances in $1\ \mu\text{m}$ CMOS integrated circuits. The dimensions are approximately to scale. (From Yang and Chatterjee [47], slightly modified)

1.4 Interconnect Modeling

MOS VLSI circuits consist almost entirely of MOS transistors and their interconnections. In a typical MOS VLSI chip, active device area is 10% while the physical area occupied by interconnect and isolation regions is 6 to 10 times the active device area. For this reason the role of interconnect is becoming increasingly important as the feature size is scaled down to submicron dimensions and device density is increased on the chip. Figure 1.2 shows a vertical cross-section of a $1\ \mu\text{m}$ design rule CMOS technology [47]. From this figure it is reasonable to expect that capacitive coupling between the metal lines and from metal lines to devices will play a significant role in the circuit response. In fact, interconnect capacitances are becoming dominant in determining the performance of VLSI circuits. Therefore, these parasitic capacitances must be taken into account during the chip design. The distributed resistance and capacitance of long signal lines form a low pass filter circuit which can affect signal timing. The switching power necessary to drive this interconnect loading is a significant part of the total chip power dissipation. Modeling of these interconnect properties is thus important and must be included by the designer when checking circuit performance through circuit simulation tools. The models for the parasitic capacitances and resistances, outside the device but part of the chip, are outside the scope of this book and interested readers are referred to the references cited [27], [48].

1.5 Subjects Covered

In this book we will cover analytical models for MOS VLSI devices and their model parameter determination. Emphasis will be on models that are suitable for VLSI circuit simulation. Although models discussed will be based on device physics, these models will often include empirical factors in order to account for the second order effects essential to model short geometry device behavior.

The basic semiconductor and *pn* junction theory essential for the development of the MOS transistor models are reviewed in Chapter 2. The overview of MOS transistor operation and characteristics are discussed in Chapter 3. Also included in this chapter is the overview of VLSI MOSFET characteristics such as MOSFET scaling, hot-electron effects, and MOSFET parasitic elements. The MOS capacitor, which is used for the characterization of MOS process and is basic to understanding MOSFET operation, is the topic for Chapter 4. From a circuit modeling point of view, MOSFET threshold voltage is the single most important device parameter. The threshold voltage models for large and small geometry MOSFETs are developed in Chapter 5. The device DC models are discussed in Chapter 6 while AC models, both small and large signal, are covered in Chapter 7. Models for hot-electron effect, particularly substrate and gate current models, and device life-time models are covered in Chapter 8.

The experimental setup, required for taking device data for different geometries and as a function of bias, is discussed in Chapter 9. Methods of determining some basic parameters such as threshold voltage, mobility of the carriers in the inversion region, doping profile, MOSFET capacitance measurements etc. are also covered in this chapter. The general purpose nonlinear optimization techniques for model parameter extraction are discussed in Chapter 10. The MOSFET model parameter extraction in general are also covered in this chapter. Since SPICE is used extensively through out the industry and at various universities, we have devoted Chapter 11 to the Diode and MOSFET models and their parameters as implemented in Berkeley SPICE. Finally the statistical variations of the MOSFET parameters due to the process variations are covered in Chapter 12.

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