Chapter 1

BSIM and IC Simulation

BSIM (Berkeley Short-channel IGFET Model) became the first international industry standard compact model for the simulation of CMOS (Complementary Metal-Oxide-Semiconductor) integrated circuits in 1997. It is believed that most of the ICs developed worldwide since 1998 were designed using BSIM. BSIM has served a wide range of CMOS technologies and IC applications.

1.1 Circuit Simulation and Compact Models

An integrated circuit contains millions to billions of transistors. The functionality and performance of the circuits must be verified by computer simulation before it is committed to expensive fabrication. Circuits are simulated by a method known as SPICE (Simulation Program with Integrated Circuits Emphasis), which was first developed by Professors Ron Rohrer and Don Pederson and their students at the University of California, Berkeley, in the early 1970's. In this method, the differential and algebraic nodal and branch equations (DAE) of an integrated circuit are solved by numerical analysis algorithms. The circuits are usually nonlinear because transistors such as MOSFETs (Metal-Oxide-Semiconductor Field Effect Transistors) are nonlinear devices (in contrast to a bias-independent resistor or capacitor).

For MOSFET devices, the complex behavior of the transistor drain current of the general form of $I_d(V_g, V_d, V_s, V_b, L, W)$ is accurately represented by a group of analytical equations known as a compact model. If these equations are printed on paper, they may occupy a few pages. However, when they are implemented in SPICE, tens of thousands of computer code lines result. The length and complexity of the functions used in the equations have significant impact on the circuit simulation time. It is therefore important to optimize both the computational efficiency of the model and its accuracy. In addition to the drain current, the device terminal charges and/or capacitances are also represented by analytical equations.

The model equations inevitably contain many adjustable constants known as model parameters. They are adjusted by modeling engineers to fit the compact model to measured terminal currents, conductances, charges and capacitances of the transistors — a process known as model parameter extraction. This process is performed with the aid of extraction software tools.

Large circuits are designed sometimes by using what is called cell library methodology. A circuit is often assembled from a pre-selected and characterized library of building blocks known as standard cells. A standard cell library typically contains many hundreds or thousands of standard cells such as inverters, NOR and NAND gates, flip flops, as well as other more complex cells. Every cell is characterized with SPICE simulation and compact models. The simulation results are reduced to a macro model – Often an expression of input to output delay, power dissipation, noise, and circuit gain as functions of input voltage ramp rates, frequencies, load capacitances, device parameters, supply voltages, and temperatures.

In other cases, circuits are simulated and designed with SPICE and compact models directly. For instance, an entire memory chip may be simulated with SPICE. Very often, large circuits are divided into smaller blocks each containing hundreds or thousands of transistors for SPICE simulation in order to complete the circuit simulation in hours rather than days or even weeks. In order to speed up the simulation of even larger circuits including SRAM memory circuits, another class of SPICE, “fast SPICE simulators”, are utilized to obtain satisfactory accuracy but with only a fraction of SPICE simulation time. This is accomplished with a combination of techniques including circuit partitioning and building table models of transistor characteristics rather than evaluating the equations of the compact model for every iteration at every time point. However, tables are still built from model equations. Therefore, nearly all ICs are designed with the use of transistor compact models.

1.2 BSIM – The Beginning

BSIM stands for Berkeley Short-channel IGFET Model. IGFET (Insulated-Gate Field Effect Transistors) is an older, more generic name for MOSFET transistors. BSIM's genesis can be traced back to 1984 [1 – 2]. This work produced BSIM1. Later Min-Chie Jeng working with Ping Ko and Chenming Hu introduced a successor version BSIM2 [3].

Hu and Ko had a close research collaboration in MOSFET physics and technology. The BSIM research was funded by the Semiconductor Research Cooperation (SRC), a consortium of semiconductor companies that funds university research projects deemed important to the IC industry. Their research into the more fundamental device physics and behaviors of advanced MOSFETs attracted additional industry supports. In this way, they gradually built a collection of models for the V_{th} (threshold voltage) dependence on biases and gate lengths, mobility degradation, velocity saturation effects, output conductance, unified flicker noise theory, SOI, and gate tunneling leakage. Eventually, these models became the building blocks of later BSIM models.

1.3 BSIM3 – A Compact Model Based on New MOSFET Physics

Most IC simulations require the accuracy to be better than a few percent from linear to saturation and from subthreshold to strong inversion covering a current range from pA/μm to mA/μm. This accuracy is achieved by painstaking modeling of many physical phenomena in a modern MOSFET including electrostatic, materials, quantum, and thermal effects. When another student Jian-Hui Huang started to work on a new version of BSIM around 1991, it was decided that the new version would incorporate some of the new original physical models mentioned in the previous sub-section. This approach was a marked departure from all previous compact models. Those models opted for simple equations favoring the reliance on "fitting" the transistor data to simplistic model equations over the use of physical, predictive, and complex models. The decision was a gamble that physics-based models can justify the model computational cost with their better accuracy and robustness. This new approach began modestly with more accurate models of V_{th} and the drain saturation voltage, V_{dsat} [4] and an accurate model of the output conductance of MOSFETs [5]. The output conductance is very important to the accurate simulation of analog circuits because it determines the voltage gains of amplifying circuits. The result was BSIM3 [6]. BSIM3 was soon recognized as being far superior to the other compact models of that time.

For example, the output conductance is no longer explained by just channel length modulation but two additional mechanisms — drain-induced barrier lowering (DIBL) and hot carrier induced body bias effects [5]. Each of these three mechanisms in turn is modeled with insights derived from research on the quasi-two-dimensional analysis of the velocity saturation region near the drain [4], the effect of channel length and drain voltage on the threshold voltage [7], and the hot-electron current [8]. For the first time, a compact model can model the output conductance in a way that is not only accurate but also predictive of the effects of changing the gate oxide thickness, junction depth, and the threshold voltage. On the other hand, Reference [7] is the basis of BSIM3's predictive V_{th} roll-off model, and Reference [8] is the basis of the substrate current model.

Another example is the gate induced-drain leakage or GIDL [9], the band-to-band tunneling current induced by the gate-to-drain voltage V_{gd}. Once the mechanism was clearly understood, a simple analytical model became obvious and proved to be accurate.

Yet another example is the flicker noise or 1/f noise. The unified flicker noise model incorporates both the fluctuation in the number of inversion layer charge carriers (the number fluctuation) and the fluctuation in the Coulombic scattering mobility (the mobility fluctuation). They are correlated because both are caused by the fluctuation in the number of trapped charges in the SiO_2 near the silicon/SiO_2 interface [10]. This model was characterized in detail using the random telegraphic noise measurements that can only be observed in transistors with very short lengths and narrow widths such that a transistor may contain only one or two oxide traps [11]. These physics studies led to an accurate compact model of the MOSFET flicker noise [12].

1.4 BSIM3v3 – World's First MOSFET Standard Model

BSIM3 was released in 1993. In that year, Ko moved to Hong Kong but stayed involved with BSIM for several more years. Hu continued to improve the physical accuracy by modeling poly-silicon depletion, universal mobility based on V_{th} and the gate voltage V_{gs} [13]. More important, the subthreshold and inversion regions of operation are now modeled with a single continuous function, V_{gsteff}. Verified with careful split-capacitance measurements, this model was a major improvement [14]. Similarly the linear and saturation regions are modeled with a single function, rather than piecewise formulations in practice then, through a continuous effective drain-to-source voltage V_{dseff}. These changes eliminated glitches in high-order derivatives of MOSFET drain current.

Encouraged by the early favorable reactions from the industry, BSIM3 began to emphasize robustness and usability for various CMOS technologies. BSIM was to be maintained and supported as a tool that billion-dollar companies may depend on for operation. In other words, impact to the industry joined creation of knowledge as an explicit goal of the BSIM project. Efforts were made to scrub thousands of lines of C-code for possible occurrences of numerical problems such as divide-by-zero, square-root-of-negative, round-off, discontinuities and over/under-flows that would cause circuit simulation to abort. It also meant timely releases of bug fixes and active communications with users via numerous emails and the BSIM release website, http://www-device.eecs.berkeley.edu/~bsim3/. BSIM3v3 won the R&D 100 Award from the R&D Magazine as one of the most significant R&D products of 1995. These efforts culminated in a robust productized release of BSIM3v3 [15, 16, 17].

The semiconductor foundry industry was beginning to grow. A foundry gives its customers, the circuit design companies, basically these inputs to undertake the design process: Compact models such as BSIM, a set of geometrical and electrical design rules, and reference design flows. The foundry is then obligated to deliver working products of the designs that the customers may create with these inputs. To both parties, a very close agreement between the models and all the behavioral details of transistors is of paramount importance. One practical way to eke out the last few percents of accuracy is a pedestrian technique called binning, making model parameters themselves functions of transistor channel lengths and widths, such that a single set of model parameters can apply to all transistors manufactured with the same process recipe.

Inspired by the success of BSIM3v3, several companies started to organize a movement to standardize a compact model. The purpose was to promote the adoption of a standard model by the IC industry. At that time, most large semiconductor companies developed their own transistor models. Often a single company would have many models in active use at the same time. Smaller companies would license models from CAD tool companies. There were many dozens of MOSFET models in use and the resources expended by each company to maintain these models and to fit each new generation of transistors to multiple models were enormous. This problem was aggravated by the dual trends of increasing inter-company and international collaborations and the growing foundry-fabless business model. Both trends would be well served if all the companies use the same model.

In 1996, Sematech, another semiconductor industry consortium, organized a series of workshops to discuss whether and how to select a standard model. This led to the formation of the Compact Model Council (CMC) that defined and executed the year-long process of selecting an industry standard MOSFET model. Several models competed in the selection process. In 1997, BSIM3v3 was selected by CMC as the world's first standard transistor model for IC simulation. The industry rallied around BSIM. Since then, BSIM3v3 has been employed for the 0.5μm, 0.35μm, 0.25μm, 0.18μm, and 0.15μm technology nodes.

1.5 BSIM4 – Aimed for 130nm Down to 20nm Nodes

BSIM continues. With the release of BSIM4 [18] in 2000 by Weidong Liu, Xiaodong Jin, Kanyu M. Cao, and Chenming Hu, BSIM was able to support the sub-130nm CMOS technologies and the growth of high-speed analog, mixed-signal, as well as radio-frequency (RF) CMOS integrated circuits that powered new lifestyle including wireless applications of the 21st century. A major new model is the physical holistic noise model for the channel thermal noise and the induced gate noise [19, 20]. The induced gate noise and its correlation with the channel thermal noise are modeled. Accuracy at high frequencies up to the cut-off frequency of transistors is achieved with a simple intrinsic input resistance (R_{ii}) model. A substrate resistance network was added. A novel quantum effect model called the charge layer thickness model was introduced [21]. The first gate direct-tunneling leakage current model was also introduced to anticipate the rise of gate leakage currents [22]. The pocket implant effect in advanced MOSFETs was introduced [23]. The layout-dependent effects from mechanical stress and well proximity were modeled. The modeling of high-*k* metal-gate stacks and non-silicon materials became possible. BSIM4 has been used for the 0.13µm, 90nm, 65nm, 45/40nm, 32/28nm, and 22/20nm technology nodes.

1.6 BSIM SOI

In parallel, the BSIM team developed a compact model for SOI-MOSFETs, BSIMSOI. Naturally, BSIM SOI shares many features and model modules from BSIM3 and BSIM4. It took major efforts to develop a floating-body model [24] as well as a self-heating model [25, 26], which required the use of a thermal sub-circuit to model the history dependencies of the underlying physical phenomena. BSIM SOI has served several major semiconductor companies for SOI-CMOS IC products.

1.7 Impact of BSIM

Upon the selection of BSIM as the industry standard model in 1997, all the foundry companies quickly adopted BSIM. This led to hundreds of fabless companies to design all their products using BSIM since then. Gradually, integrated design-manufacturing (IDM) companies gave up their own proprietary compact models and migrated to BSIM. A few companies continued to use their own proprietary models but also used BSIM so as to facilitate the collaborations with other companies.

Most of the ICs using 0.5μm and newer technologies since 1997 were designed with BSIM. That amounts to a trillion US dollars worth of ICs.

1.8 Looking Towards the Future – The Multi-Gate MOSFET Model

As the CMOS technology continues to scale down, the device drain terminal is pulled closer to the middle of the channel. This increases the capacitive coupling between the drain and the channel, producing unwanted/unduly short-channel effects such as standby channel leakage currents. This is the biggest problem facing the nearly five-decade long planar CMOS transistor structure.

FinFETs [27] allow the gate to control the channel from three sides of the channel, hence the term CMG (common multiple gates), which increases the gate control and allowing the gate length to be further scaled down. Since the introduction of FinFETs, this structure has set the world's records of the smallest gate length several times at various research laboratories. The current record is held at three nanometers.

BSIM-CMG [28] is a compact model for the class of common multi-gate FET devices. This model has been extensively validated with advanced multi-gate CMOS technologies, both SOI and bulk. It is reviewed as an example of a compact model to serve multi-gate CMOS technologists and circuit designers to facilitate the transition from the planar CMOS to the multi-gate vertical CMOS era.

1.9 The Intent of This Book

Modeling ideal prototypical CMOS devices well is one thing, but modeling myriad real devices of numerous technology generations well is the hallmark of BSIM. BSIM4 is no exception and it is by far the most sophisticated and widely used compact MOSFET model. It has served innumerable device technologists, design automation engineers as well as IC designers around the world for half a dozen CMOS technology nodes.

This book is intended to present and analyze in depth the BSIM4 theory, hands-on techniques, and methodology that can take a compact model from its prototype into a production-worthy version. It covers MOSFET device operation and physics, manufacturing process effects, model formulations, parameter extraction, SPICE implementation, and their implications to integrated circuit design.

This book is written for BSIM users, undergraduate and graduate students in EE, and those that make their professions in those areas.

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