Foreword

This monograph is the seventh book in this series on modeling of integrated-circuit devices. The purpose of this series is to provide archival references, described by the model originators or authorities, on the mathematically compact and computationally efficient engineering models of transistors and devices that are interconnected on a small, about a square centimeter or smaller area, silicon semiconductor wafer, die, dice, or chip, containing many integrated transistor circuits, which is the 'brain' of the equipment used in our daily activities today.

The monograph series idea came about six years ago in 2005 when I was asked by colleagues of Compact Modeling Council and Compact Model Community (CMC) to join them and give a keynote at their 4th annual international Workshop on Compact Modeling on May 10, 2005. I had been absent on transistor modeling research for 40 years since my first PhD student, Henry Pao, finished his PhD thesis in 1966 on the analytical model of the surface-channel silicon field-effect transistor (FET) with the Metal-Oxide gate on Silicon body (MOS). The prerequisite was to talk about a subject of their prime interest. But, I had not heard the term "compact model" and had the faintest idea of its meaning due to 40 years of absence. While searching the literature for references to write the keynote address, it became evident that there were many compact models and originators, but few books had provided descriptions sufficiently detailed for the professionals who must use the compact transistor models to execute a computer-aided-design of the integrated circuits that contain thousands to millions, now more than a billion transistors. A second purpose of this device modeling series is to provide state-of-the-art textbooks for graduate students and reference books for practicing engineers who are the users but may not be the designers of the latest integrated circuits.

After editing six compact modeling monograph volumes in this ASSET (Advances in Solid-State Electronics and Technology) series and reading literature on the faster-than-exponential rise of progresses in other areas of sciences and engineering, it seemed suddenly becoming obvious, if not already a common knowledge, that the word 'Model" is the buzz word everywhere. So perhaps it is timely to add a few words in this "Foreword of Opportunity" about "Model", because in the two 60+year-old transistors which dominate everything of our life today, and even earlier devices, "model" has been the key to their discoveries and inventions. Quantitative modeling was certainly used even earlier in all engineering; even earlier, in evolution, in qualitative and habitual learning, and in the basics of the most basics of foundation of physics, explored by man about his origin and universe.

Our past, present and future are all model based. Some are more quantitative, others more qualitative; some more deterministic, others more statistical; some local, others global; some experience based, others more science (scientific method) based. Weather, archeology, evolution, particles and materials, societal and custom-habit, stock market, biology and medicine, are some of the examples, in addition to the engineering feat, the invention on paper, of the two transistors by Shockley (see below). Most were compact or incomplete models based on a limited set of inventors' then current and latest knowledge, idea, notion, and imagination. All were already abbreviated or compact, compacted from the 'complete' theory based on intuitive physics, but most were further compacted to meet mathematical tractability by the inventor's own mathematical skill if not more so the inventor's desire to popularize the invention in laymen or more common language rather than abstract-obscure. But the compact models or compact-compact (compact^2) models are increasingly less compact or increasingly more complicated because of increased computer capability to numerically solve them fast, due to better models that help design faster computers, creating still better models, a regenerative positive feedback loop. Such a loop fuels the increasingly faster than exponential rate of technology growth and advances, which would extrapolate to reach infinity at some finite future time, if not for some unseen, not modeled missing resistive-damping.

This book volume on the MOS transistor compact model BSIM exemplifies the development of a compact model, in this case, the one most used by man in its successful engineering applications on the design of computing, communication, and control circuits, which process electrical signals. BSIM is a compact model on the field effect transistor with insulated gate, the Insulated Gate Field-Effect Transistor (IGFET), more commonly known as the Metal-Oxide-Silicon field effect transistor (MOSFET) or just MOS Transistor (**MOST** which drives home the fact that it is the **most** abundant artificial device produced by man). The models or mathematical models for transistors are based on the current knowledge in the physics and 'model' of matter, the condensed phase which semiconducts electricity by two species of carriers or 'elementary' particles, electrons and holes, with exactly opposite unit of electrical charge, but somewhat different in their inertia masses, not unexpected in this imperfect world and asymmetrical, skewed universe, not unlike the two biological genders of much larger size, containing many more molecular particles.

Field effect transistor (FET, 1952) is one of the two transistors invented by William Shockley about sixty years ago. The other was the bipolar junction transistor (BJT, 1949). In-between, he wrote his classic textbook, *Electrons and Holes*. The two transistors have been the foundation devices of the electronic revolution. Shockley invented them on paper using the simplest physics models, one current channel in each, the diffusion current for the BJT and the drift current for the FET, both in the bulk or bulk-channel of a semiconductor, the Germanium, because crystalline Silicon was difficult to produce in the 1950's due to its high melting point, 1420C, even at the Bell Telephone Laboratories. The complete transistor model, which became obvious to this author not until 60 years later, is the eight channel device, analyzed by this author and his collaborator, Jie Binbin, both at Xiamen University, China, which is the eight combinations of electrical current channels, the drift and diffusion currents of electrons and holes in the surface and the bulk-or-body channels, giving $2 \times 2 \times 2 = 2^3 = 8$ electrical current channels or electrical charge carrier transport pathways. The two foundation transistors, BJT and FET, could not have been invented if Shockley had not mentally visualized and singled out the two simplest (or most compact) models:

bulk drift (for FET) and bulk diffusion (for BJT) by just one carrier species (electron or hole), that enabled him to mathematically analyze and design the two transistors and to predict their electrical characteristics and performance, all on paper, 60+ years ago.

The comprehensive and authoritative compact modeling of the modern BJT was covered by the latest prior volume of this compact transistor model series, known as the HICUM, authored by Professor Michael Schroter of Germany and Dr. Anjan Chakravorty of India, and published by WSPC of Singapore in the fall of 2010.

The compact modeling of the second transistor type, FET, invented by Shockley in 1952, in the modern form, the silicon MOSFET or silicon MOST, is covered in this volume. The model is known as BSIM, and is in its fourth generation, BSIM4. It is authored by the founder-inventor of the BSIM, Professor Chenming Hu of China and USA, and his able assistant, Dr. Weidong Liu of China and USA. It is published in this ASSET series (this book) by WSPC one year later in the fall of 2011.

The publication sequence of these two volumes on the two transistors, 1949-BJT and 1952-FET in the modern form of Si MOST, followed the invention and the application histories of the two transistors. But this coincidental publication sequence was not planned in this compact modeling monograph series; however, the publication sequence does reflect the volume manufacturability determined by the advances of fabrication technology, especially the equipment, which also determines the application volumes and varieties.

I am especially thankful to the invited authors of the four startup volumes (Narain, Carlos+Márco, Mitiko+Hans+Tatsuya, and Arjun), of the later volumes (Cherming, Michael+Anjan, and Chenming+Weidong of this volume), and of the two to be published volumes (Ching-Hsiang+Yuan-Tsai and Francisco+Adelmo.). They concurred with my objectives and agreed to take up the chore of writing their books during their very busy schedules. Some have delays of one, two or even three years. Nevertheless, their monographs are still the archival records of the state of the art, and the world's authoritative contributions to the device modeling literature, because these authors are the creators, inventors and/or authorities of the models, and because the models are the industry-wide consensus models, used by all circuit designers of recent generations, and expected to be used by the future generations.

The present volume is a detailed comprehensive description of the latest version of the industrial consensus compact model for silicon MOSFET, the BSIM4, used by 90% if not 95% or more of the integrated circuit design and application engineers, and learned by all the electrical and computer engineering graduate students, for generations, two if not more decades. It also contains the historical development from the first BSIM, narrated by its creator, innovator, custodian, and father, Hu Chenming or Calvin Hu, the TSMC Distinguished Chair Professor at the University of California, Berkeley. A most important and salient teaching feature of this book is that the compact model of each of the electron-hole transport phenomena in the MOSFET is developed from the basic device physics of charge carrier transport in semiconductors, governed by the Shockley Equations. The compacted models are not only accurate in device physics, but also in computational efficiency and accuracy to give the numerical results for representing the characteristics of the transistor which must be provided to the circuit simulator, such as SPICE, to analyze the performance of an integrated circuit, which may contain hundreds to millions of transistors, exceeding one billion recently. The fastest and largest (in memory capacity) computer would not be able to give numerical results in a short enough turn-around time (say a day or even a week) for manufacturability if the one million or more transistors were represented by their original and not-compacted models.

The last chapter gives the current and latest compact model for the upcoming generation of sub-quarter-100nm or 20-nm MOS transistor using the 3-dimensional Fin-like geometry structure, known as the FinFET, invented by Professor Hu.

The notations and terminologies employed in this monograph follow the industrial practice used by the design and manufacturing engineers of the MOSFETs. The monograph descriptions provide the connection of the notations and terminologies to the physics of semiconductors. For examples, silicon bandgap is noted as electron energy gap in silicon; avalanche multiplication and breakdown, as interband impact generation of electron-hole pairs by hot or energetic electron or hole; flicker noise, as 1/f noise from the addition of many trapping noise sources each with a different trapping time constant; white noise or Johnson noise, as random scattering noise with a reciprocal scattering rate in femto second range so the 'corner" or noise-power drop-off frequency is in the THz range; and many others.

I would like to thank all the WSPC production staff members at Singapore and their production editor of this monograph, Mr. Tjan Guangwei, and the acquisition editor, VP Ms. Zhai Yubing in New Jersey, for their untiring and dedicated efforts and supports. Special thanks are due NTU Physics Professor Kok-Khoo Phua, the Founder and Chairman of WSPC, for his farsights and foresights, one of which was pursuing me into authoring and editing textbooks and monographs in 1990, when I was rather discouraged if not also disgusted by the tactics of some publishers, which is a proof of my thesis, the Evolutionary Intelligent Design. I also thank Dr. Jie Binbin, Professor of Physics of Xiamen University, for editorial assistance. We also thank our supporters, President Zhu Chongshi, School of Physics Dean Wu Chenxu, and Department of Physics Chair Zhao Hong, all of Xiamen University, China. Finally, the editorial efforts of both of us, Sah Chihtang and Jie Binbin of this ASSET series, have been supported by the CTSAH Associates, Florida, USA, which was founded by the late Linda Su-Nan Chang Sah in mid-1970 at Urbana, Illinois, and which was reactivated on February 27, 2010, at Gainesville, Florida.

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Initial draft, July 1, 2011, near the North Pole on way to
Beijing and Xiamen from Seattle on Delta B767-300ER.
Final version, July 4, 2011 at Yi-Fu Hotel, Xiada campus.
Eighth year on August 13, 2011 and moving forwards.