

# Foreword

The idea of a monograph series on compact transistor modeling came about when I was looking into the literature to write the keynote address, on the history of MOS transistor compact modeling, invited by the Founder of the Workshop on Compact Modeling, Professor Xing Zhou of Nanyang Technology University, and his program committee, to be presented at its 4<sup>th</sup> Workshop on May 10, 2005. The purpose is to provide an archival reference series, described by the originators or the veterans, of the compact models of the MOS and bipolar-junction transistors and passive components. A second purpose is to serve as textbooks for graduate students and reference books for practicing engineers, to rapidly disseminate to them the detailed design methodologies and underlying physics, in order to meet the ever faster advances in the computer-aided-design of integrated circuits containing thousands to billions of silicon semiconductor MOS and bipolar-junction transistors, passive diode components (capacitors, inductors, resistors), and interconnects. It is also the objective of this monograph series to provide timely updates via website and internet exchanges between the readers and authors, for public dissemination, and for new editions when sufficient materials are accumulated. I am especially thankful to the invited authors of the four startup and later monograph volumes who concurred with me and agreed to take up the chore to write their books.

It is most timely to document the second generation compact MOS transistor model, evolved from my 1964 threshold-voltage model to my 1966 surface-potential model that is being employed by the circuit design engineers to simulate the transistor and by the foundries to fabricate integrated circuits in this decade and beyond. This monograph is a device-physics-based in-depth description of one of the three industry-consensus compact MOS transistor models. It is known as HiSIM, developed by Professor Mitiko Miura-Mattausch, her two collaborators, Professor Hans Jurgen Mattausch and Assistant Professor Tatsuya Ezaki, and her graduate students and industrial associates at the Hiroshima University in Japan. We are extremely pleased to publish this timely monograph to serve as a reference for practicing engineers and a textbook for graduate students. Its depth and thoroughness provide the clarity and rigor to grasp the approximations that are necessary to compact the MOS transistor model for simulation of integrated circuits containing thousands to billions of MOS transistors.

I would like to thank all the WSPC editors and this monograph volume's copy editor Mr. Tjan Kwang Wei (Tjian Guangwei) at Singapore and the acquisition editor Dr. Yubing Zhai at New Jersey, for their and her timely efforts, and Professor Kok-Khoo Phua, Founder and Chairman of WSPC whose support and publishing philosophy have made all these possible. I am also indebted to Professor Binbin Jie of Peking University for his helpful efforts as my collaborator and also personal assistant, without which my reentry into device modeling would not have happened after 40 years of absence since writing the threshold-voltage and then two surface-potential-based MOS transistor modeling articles in the IEEE Electron Devices in 1964 and 1966. I also acknowledge my late wife Linda Su-Nan Chang Sah for founding the CTSAH Associates in the 1970's to provide me the financial independence to undertake engineering and science investigations in later years, and her younger brother Fred Tsang and our children, Dinah and Robert Sah for their continued technical supports and mental encouragements.

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