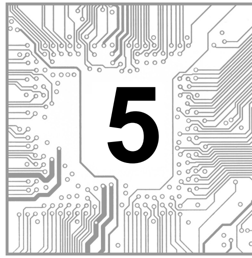

Insulated-Gate Bipolar Transistor

5.1. Introduction

MOSFET devices have been widely used since 1970s for various electronic signal and power applications. For power switching applications, there exists the requirement for the device to sustain a high operating voltage, e.g. a few hundred volts. This is made possible by placing a thick and lightly doped drift region as an extension of the MOSFET drain emitter to accommodate the field depletion. By doing so, the penalty on the device will be having a higher on-state conduction resistance as the MOSFET current conduction is made of majority carrier transport, and the conductivity modulation occurred in the drift region by the majority carriers is normally insufficient. In 1980s, a new type of device named insulated-gate bipolar transistors (IGBT) was invented to improve the situation. By its operational principle, the device is a MOS-driven power bipolar device which has both types of carriers flowing in the drift region to lower the conduction resistance. The device has been known earlier by many different names such as, the insulated-gate rectifier (IGR) (Baliga *et al.*, 1982), insulated-gate transistor (IGT) (Chang *et al.*, 1983, 1984), conductivity-modulated field-effect transistor (COMFET) (Russell *et al.*, 1983; Goodman *et al.*, 1983), and bipolar-mode MOSFET (IGBT) (Nakagawa, 1984). For such a MOS-driven power bipolar transistor, it combines the advantages of both the MOSFET gate control and the nature of bipolar transistor into a single device. Due to the high-impedance characteristic of its MOSFET input gate, the driver circuitry for the IGBT is essentially similar to that for the power MOSFET. With the key feature of having bipolar conductivity modulation in the lightly doped drift region, it lowers the on-state power dissipation for devices of high-voltage rating. However, the bipolar excess carriers needed for low on-state conduction voltage do make the device turn-off speed much slower than that

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of the power MOSFET of similar current rating. The IGBT device exhibits a current tailing, e.g. in sub-microseconds range, during turn-off which restricts the device to operate at high switching frequency. Carrier lifetime control is then needed to improve the situation.

The IGBT device offers a good solution to medium-range frequency (e.g. $<$100 kHz), high-voltage high-current switching applications. Under special switching techniques, such as zero current switching resonant converters, the IGBT has been shown to operate in the hundreds of kilohertz range (Rangan, 1987). It has been shown theoretically and experimentally that the p-channel IGBT can have performance characteristics comparable to those of n-channel IGBT (Chang *et al.*, 1984), thus allowing the use of complementary devices in power electronics applications. Also, the IGBT device can handle a larger current density compared to the power bipolar junction transistor (BJT) and the power MOSFET. For example, at a breakdown voltage of 600 V, the IGBT device carries a current density at about 20 times that of the power MOSFET and at about five times that of the power BJT. However, the presence of a diode knee voltage in its current–voltage characteristic prevents the IGBT device to be used in applications that require a very low forward voltage drop. Since 1990, IGBT devices of voltage ratings between 600 and 1200 V have been commonly used in power conversion applications. Voltage ratings of 2500 V and above are also recently available in the market.

In power electronic circuits, it is possible to directly replace a power MOSFET by an IGBT to improve the conduction efficiency (but be careful on the long turn-off time). In general, an IGBT has a smaller die size than a similarly rated power MOSFET. Since the cost of a device is partially related to the silicon die area, the smaller die size of the IGBT makes the device a lower cost solution compared to the power MOSFET at similar current rating. Also, the IGBT device is ideally suited for inductive switching owing to the uniform current distribution in the device during turn-off. However, the device has two disadvantages in comparison to the MOSFET counterpart. First, is its slower switching speed due to the bipolar transistor structure, and the second one is prone to parasitic thyristor latch-up when operating at high current or high *dv/dt* power switching conditions.

In this chapter, the fundamental structure of the IGBT device is described along with its current–voltage characteristics. The device characteristics on switching and temperature effect are also described. This is followed by the introduction of lateral IGBT structure, integrated current sensor, and over-current protection. Other related types of MOS-controlled bipolar devices are generally described at the end.

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5.2. Device Structure and Current–Voltage Characteristics

The device structure for IGBT is similar to that of a double-diffused MOSFET (DMOS) with the exception of having the p^+ substrate (anode) for the IGBT device as shown in Fig. 5.1. As such, it is a four-layer structure that resembles that of a thyristor. Unlike the thyristor where the device latches, an IGBT is designed to turn on without any regenerative action and the MOS-gate remains in control. A wide-base p–n–p structure is formed at the bottom three layers with the p^+ substrate as the emitter, the n^--drift layer as the base, and the p-body of the MOSFET as the collector region. As such, the thickness and doping density of the n^--drift layer determines the breakdown voltage of the device. To follow the convention of the four-layer structure, the top n^+ source is named as the cathode while the p^+ substrate is the anode for the IGBT device in this chapter.

Except the leakage current, there is no visible current-flow when a negative voltage is applied to the anode with respect to the cathode because the junction between the p^+-body and the n^--drift layer is reverse-biased. The IGBT is now operating in its reverse blocking mode with the *I*–*V* curve as shown in Fig. 5.2. Most of the depletion region is extended into the lightly doped n^--drift layer. The reverse blocking voltage is essentially the BV_{CBO} of the p^+ substrate/n^--drift/p-body transistor. As such, the doping and thickness of the n^- layer are chosen to yield the desired blocking voltage. It should be noted that a proper junction edge termination and passivation technique

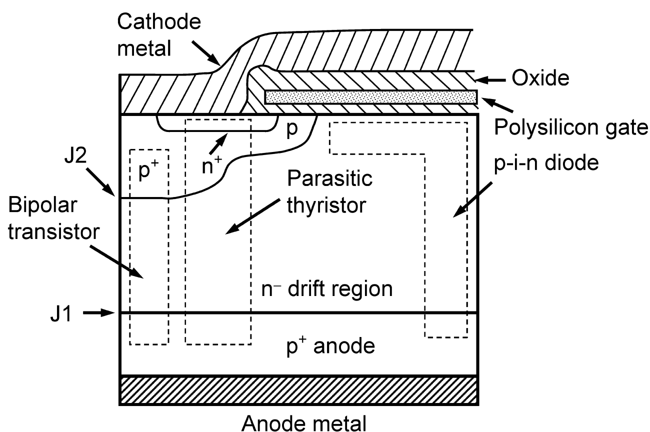

Fig. 5.1. Device structure of an IGBT device.

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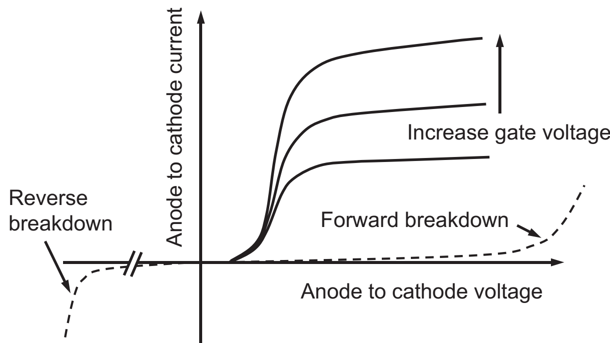

Fig. 5.2. Forward and reverse blockings (dash lines), and forward conduction *I–V* curves (solid lines) of an IGBT device.

must be employed to achieve the optimum reverse blocking voltage. When a positive voltage is applied to the anode terminal, with the gate shorted to the cathode (ground) terminal, the IGBT is operating in its forward blocking mode since the junction between the p-body and n^--drift region is reverse-biased. The IGBT device is said to operate in its forward conduction state if a gate voltage of greater than the threshold voltage is applied under positive anode-to-cathode bias condition. Similar to the MOSFET device, a conductive channel is induced underneath the oxide gate in the p-body region. Electrons flow from the n^+-cathode to the n^--drift region while the p^+ substrate injects holes into the n^--drift layer region to form the bipolar conductivity modulation in the drift region. The *I–V* curves for various gate voltages are shown in Fig. 5.2. The injected hole concentration increases as the anode-to-cathode voltage increases. Thus, the forward current of the IGBT increases similarly to that of a p–i–n diode. The forward current starts to saturate when a significant voltage drop develops across the MOSFET conducting channel in the p-body region. These current–voltage characteistics are similar to those of a power MOSFET, except for the presence of the diode knee voltage at the starting point of current conduction.

In applications where the IGBT device is not required to block a reverse voltage, an asymmetrical IGBT structure is formed with an n-buffer layer placed between the p^+ substrate and the much lightly doped n^--drift layer as shown in the lower part of Fig. 5.3. In the symmetrical structure as shown in the same figure, the doping density and thickness of the n^- layer are chosen to prevent punch-through to the p^+-anode of the IGBT. In the case of the asymmetrical IGBT structure which is a classic punch-through structure, the electric field distribution changes from the triangular shape to the rectangular-alike

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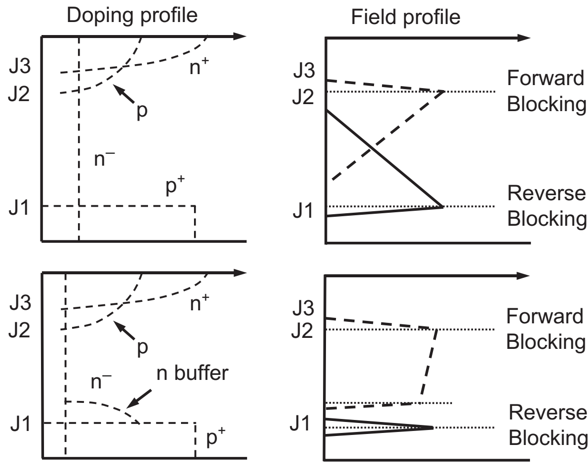

Fig. 5.3. Symmetrical (upper) and asymmetrical (lower) IGBT device doping profiles and the field distributions.

shape. Thus, the forward blocking capability of the asymmetrical device is increased approximately by a factor of 2 more than that of the symmetrical structure if a similar n^--drift layer thickness was used. Therefore, with a shorter drift region length it can be used to enhance the forward conduction characteristics. And, due to less amount of excess-charge storage, this asymmetrical IGBT structure has a lower turn-off time compared to that of the symmetrical IGBT structure.

5.2.1. Forward Conduction Characteristics

Forward conduction occurs when a positive bias is applied to the anode with respect to the cathode and with a positive gate voltage greater than the applied threshold voltage. Current flow from anode to cathode must pass through a p–n junction formed by the p^+ substrate and n^--drift region, and the MOS channel. Thus, a diode knee is present in its initial forward current–voltage characteristic as shown in Fig. 5.2. Based on the structure, the IGBT can be represented as the equivalent circuit shown in Fig. 5.4, which is a p–i–n diode in series with a MOSFET device, named as the p–i–n/MOSFET model. Or, because the IGBT device is also a MOS-driven BJT structure, it can alternatively be modeled by the BJT/MOSFET equivalent circuit as shown in Fig. 5.5 (Baliga, 1987).

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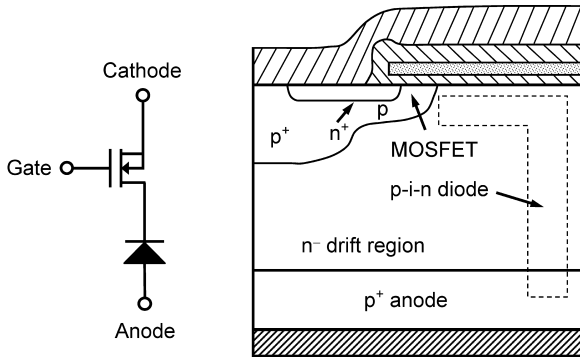

Fig. 5.4. The diode–MOSFET equivalent device model.

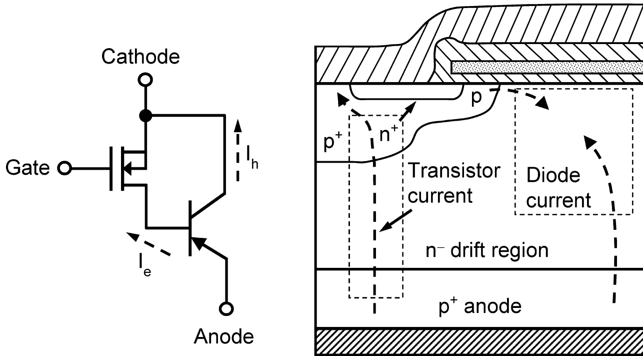

Fig. 5.5. The BJT–MOSFET equivalent device model.

5.2.1.1. *p–i–n/MOSFET Model*

The p–i–n/MOSFET model, as shown in Fig. 5.4, fully explains the presence of the diode knee of the IGBT current–voltage characteristics. At low forward biases, the current density is related to the voltage drop across the p–i–n diode by Eq. (3.56) and repeated here under medium to high forward bias condition,

$$J_{\mathrm{f,pin}} = \frac{2qD_{\mathrm{a}}n_{\mathrm{i}}}{d} F\left(\frac{d}{L_{\mathrm{a}}}\right) e^{\frac{qV_{\mathrm{f}}}{2kT}}, \tag{5.1a}$$

$$\mathrm{F}\left(\frac{d}{L_{\mathrm{a}}}\right) = \frac{\frac{d}{L_{\mathrm{a}}}\tanh\left(\frac{d}{L_{\mathrm{a}}}\right)}{\sqrt{1 - B^2\tanh^4\left(\frac{d}{L_{\mathrm{a}}}\right)}} e^{\frac{-qV_{\mathrm{n^-}}}{2kT}}, \tag{5.1b}$$

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$$B = \frac{\frac{\mu_n}{\mu_p} - 1}{\frac{\mu_n}{\mu_p} + 1}, \tag{5.1c}$$

where D_a is the amipolar diffusion coefficient, L_a is the amipolar diffusion length, μ_n and μ_p are the electron and hole mobilities in the drift region, and d is half of the drift region length. Thus, the voltage drop across the p–i–n diode can be expressed as

$$V_{f,pin} = \frac{2kT}{q} \ln \left[\frac{J_{f,pin} d}{2qD_a n_i F\left(\frac{d}{L_a}\right)} \right]. \tag{5.2}$$

For diode conduction under low bias conduction, the term *kT* shall be used instead of *2kT* in Eqs. (5.1) and (5.2), as described in Chapter 3. As the p–i–n diode is connected in series with the MOSFET, and if the upper transistor current is ignored, the same diode current will flow through the MOSFET, i.e.

$$I_{D,MOSFET} = I_{f,pin}. \tag{5.3}$$

For the MOSFET operating in its linear region, the current flowing through the device can be expressed as a function of its drain-to-source voltage drop as in Eq. (5.4):

$$I_{D,MOSFET} = \frac{\mu_n C_{ox} W}{L} (V_G - V_T) V_{DS,MOSFET}, \tag{5.4}$$

where μ_n is the effective channel mobility, $V_{DS,MOSFET}$ is the drain-to-source voltage of the MOSFET, V_T is the channel threshold voltage, L is the channel length, W is the channel width and C_{ox} is the gate oxide capacitance. From this equation, the voltage drop across the MOSFET can be expressed as

$$V_{DS,MOS} = \frac{I_{D,MOSFET} L}{\mu_n C_{ox} W (V_G - V_T)}. \tag{5.5}$$

Hence, the voltage drop across the IGBT is the sum of the voltage drops across the p–i–n diode and the MOSFET potions (Baliga, 1987):

$$V_f = \frac{2kT}{q} \ln \left[\frac{I_f d}{2qWW_d D_a n_i F\left(\frac{d}{L_a}\right)} \right] + \frac{I_f L}{\mu_n C_{ox} W (V_G - V_T)}, \tag{5.6}$$

where W_d is the effective drift region width contributed to the diode conduction. From the above equation, the p–i–n/MOSFET model characterizes the IGBT current–voltage relationship and it shows a diode knee at low forward

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current region. Just above the diode knee voltage, the current starts to increase exponentially as shown in Fig. 5.2. As the anode-to-cathode voltage of the IGBT continues to increase, the MOSFET channel eventually pinches off near the side of n^--drift region. As such, the IGBT anode current is now limited by the MOSFET channel in saturation. The collector current is now saturated and is given by

$$I_{C,Sat} = \frac{\mu_n C_{ox} W}{2L}(V_G - V_T)^2. \tag{5.7}$$

The major shortcoming of this p–i–n/MOSFET model is the omission of the hole current component flowing in the p-base region of the upper n–p–n transistor.

5.2.1.2. *BJT / MOSFET Model*

In the more appropriate BJT/MOSFET model as shown in Fig. 5.5, the MOSFET provides the base drive for the p-body/n^--drift layer/p^+ substrate BJT. The electron current component flowing through the MOSFET channel is labeled as I_e in Fig. 5.5, while the hole current component injected from the p^+ substrate into the transistor n^--drift region, of which, received by the upper p^+/cathode contact is labeled as I_h. The electron and hole current components are related by the p–n–p common-base current gain α_{PNP} as

$$I_h = I_e\left(\frac{\alpha_{PNP}}{1 - \alpha_{PNP}}\right). \tag{5.8}$$

Understand that, the current of IGBT is the sum of both hole current and electron current components. Therfore,

$$I_f = I_h + I_e = \frac{I_e}{(1 - \alpha_{PNP})} = \frac{I_h}{\alpha_{PNP}}. \tag{5.9}$$

It can be seen that the MOSFET channel current is only a part of the anode current of the IGBT. Unlike the case in p–i–n/MOSFET model, the entire anode current is assumed to flow through the MOSFET channel. The common-base current gain α_{PNP} of the wide-base lightly doped p–n–p transistor is mainly determined by the base transport factor and can be approximately given by

$$\alpha = \frac{1}{\cosh\left(\frac{L_B}{L_a}\right)}, \tag{5.10}$$

where L_B is the undepleted base region of the p–n–p transistor, or essentially the thickness of the n^--drift layer, which equal to $2d$ of the diode drift region

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length, under on-state conduction. L_a is the amipolar diffusion length at the medium and high carrier injection level. In a typical IGBT structure, the p–n–p transistor gain is about 0.5. The current–voltage relationship across the IGBT in this BJT/MOSFET model is similar to Eq. (5.6) except that the current flowing through the MOSFET is replaced by the electron current component (Baliga, 1987). Thus,

$$V_f = \frac{2kT}{q} \ln \left[\frac{I_f d}{2qWW_d D_a n_i F\left(\frac{d}{L_a}\right)} \right] + \frac{(1-\alpha_{PNP}) I_f L}{\mu_n C_{ox} W (V_G - V_T)}. \tag{5.11}$$

It is noted that the on-state voltage drop is smaller according to the BJT/MOSFET model as compared to that of the p–i–n/MOSFET model since the current flowing through the MOSFET channel is lower in the BJT/MOSFET model by a factor of $1/(1-\alpha_{PNP})$. Similarly, the saturated current is also modified accordingly

$$I_{C,Sat} = \frac{1}{(1-\alpha_{PNP})} \frac{\mu_n C_{ox} W}{2L} (V_G - V_T)^2. \tag{5.12}$$

From the above equation, the small-signal transconductance of the IGBT in the active region of operation can be derived as

$$g_m = \frac{1}{(1-\alpha_{PNP})} \frac{\mu_n C_{ox} W}{L} (V_G - V_T). \tag{5.13}$$

5.2.2. Output Resistance

In practice, an IGBT exhibits a finite anode output resistance due to (a) the reduction in effective channel length with higher anode voltage, and (b) the increase in current gain of the p–n–p transistor as its undepleted base width is reduced. Especially, a significant reduction in anode output resistance at higher anode voltage occurs in the symmetrical structure (Baliga, 1986). In the asymmetrical structure, the depletion width in the n^--layer does not change much with further increase in anode voltage because of the relatively high doping density in the n-buffer layer. Therefore, the current gain of the p–n–p transistor remains almost constant for all anode voltages. As such, the output resistance is expected to be more stable for the asymmetrical IGBT structure. The lower current gain of the p–n–p transistor in the asymmetrical IGBT structure due to the presence of the n-buffer layer also helps to keep the output resistance higher. For symmetrical structure, electron irradiation can be employed to increase the anode output resistance by lowering the carrier lifetime and subsequentially, the minority carrier diffusion length and the current gain of the p–n–p transistor can be lowered.

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5.3. Switching Characteristics

To switch an IGBT from its forward conduction state to the off-state, it is necessary to reduce the gate charge to zero in order to remove the inversion channel in the p-base region, so as to cut off the flow of electrons from the n^+-cathode to the n-drift region. After MOS-channel is turned off, the excess carriers confined in the long drift region will then slowly die down through recombination process similar to that of an open-base transistor. A current tail results as shown in Fig. 5.6. As such, the turn-off process occurs in two stages, namely immediate turn-off of the MOSFET-controlled electron current and the slow die-down of the open-base transistor (mainly) hole current.

The turn-off characteristic of an IGBT is governed not only by its internal device properties, but also influenced by the external circuitry which the device is connected to. When the gate voltage drops below the threshold voltage, the anode current reduces abruptly due to the disappearance of the MOS-channel electron current, I_e, as shown in Fig. 5.6. Meanwhile the anode-to-cathode voltage rises suddenly to compensate the reduction in the load voltage by a lower current. Therefore, the device, in particular the drift region, is now the blocking part of the supply voltage. The sudden change in the effective undepleted base

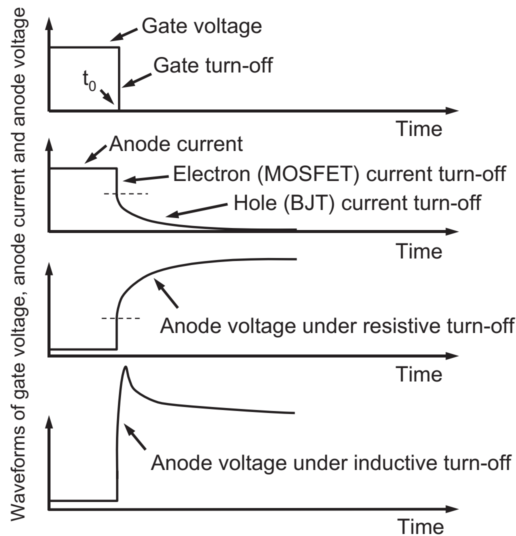

Fig. 5.6. Waveforms during IGBT turn off, namely (from top) gate voltage, anode current, anode voltage at resistive switching, and anode voltage at inductive switching.

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width will bring the current gain of the p–n–p transistor to a higher level and this will have a significant influence on the IGBT dynamic latch-up characteristics. Dynamic latch-up phenomenon will be described later. If the device is connected to an inductive load, then the voltage across the IGBT device may be much higher due to the inductive effect caused by the sudden drop of conduction current. Now, the anode current continues to flow through the device during carrier recombination process made by the high concentration minority carriers stored in the n^--drift region during on-state. Due to the relatively long minority carrier lifetime in the n^--drift region, which is necessary to achieve a low on-state conduction voltage, the current tail normally lasts for a long time which is comparable to that of bipolar devices. For this, similar methods of carrier lifetime control, e.g. proton irradiation (Mogro-Campero *et al.*, 1985) can be employed in the drift region near the p^+-anode to reduce the tail time. For the asymmetrical structure, the added n-buffer layer does provide a suitable and quicker recombination site for minority holes near the buffer region and this structure greatly reduces the turn-off tail time.

The magnitude of the abrupt drop in the anode current is determined by the amount of MOSFET electron current and is related to the current gain of the p–n–p transistor, i.e.

$$\Delta I_f = I_e = (1 - \alpha_{PNP}) I_f. \tag{5.14}$$

At the time point t_0, the hole-current flow remains the same (although the p–n–p transistor gain becomes higher at this point) as that during the on-state conduction just before turn-off. The magnitude of the transient corrector current is

$$i_f(t_0) = I_h(t_0) = I_f - \Delta I_f = \alpha_{PNP} I_f. \tag{5.15}$$

After t_0, the anode current decreases exponentially at a rate determined by the high-level minority carrier lifetime. The current waveform can be approximately expressed as

$$i_f(t) \approx I_h(t_0) e^{-\frac{t}{\tau_h}} = \alpha_{PNP} I_f e^{-\frac{t}{\tau_h}}. \tag{5.16}$$

Usually, the turn-off time is defined as the time taken for the anode current to decay to 10% of its on-state value, i.e.

$$t_{off} = \tau_h \ln(10\, \alpha_{PNP}). \tag{5.17}$$

Therefore, the turn-off time increases with the p–n–p transistor current gain and the minority carrier lifetime in the drift region.

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5.4. Latch-up

The IGBT device has an inherent four-layer thyristor structure by looking along from the p^+ anode to the n^+ cathode. Once the inherent thyristor latches up, the device will remain in its conduction state only till shut-down of the supply voltage. The MOS-gate control does not have any influence to interrupt the current conduction in the latched thyristor. Figure 5.7 shows the schematic IGBT model with the parasitic thyristor.

It is understood that, the thyristor latch-up phenomenon occurs when the sum of the upper n–p–n transistor gain and the lower p–n–p transistor gain approaches unity. We have so far studied the p–n–p transistor gain during the device on-state conduction and during turn-off operations. Here, together with n–p–n transistor gain, they will determine the operational limit of maximum on-state current conduction and the voltage–current ranges in turn-off dynamics. The latch-up phenomena can be identified in two types, namely the static latch-up and the dynamic latch-up, according to the operational status when it occurs. This is so because the transistor gain is not a constant value but a function of biasing conditions. During normal operations, the p-base/n^+-emitter junction in the upper n–p–n transistor is moderately forward-biased. This is caused by the hole current passing through the p-base to arrive at the top of cathode contact. The voltage across the junction is normally not sufficiently large to boost up the n–p–n transistor current gain of α_{npn} to a high level in order to trigger the transistor in action. In a sense, during normal IGBT operation, the top n–p–n transistor is in the dormant state, while the bottom transistor is in the active (conduction) state.

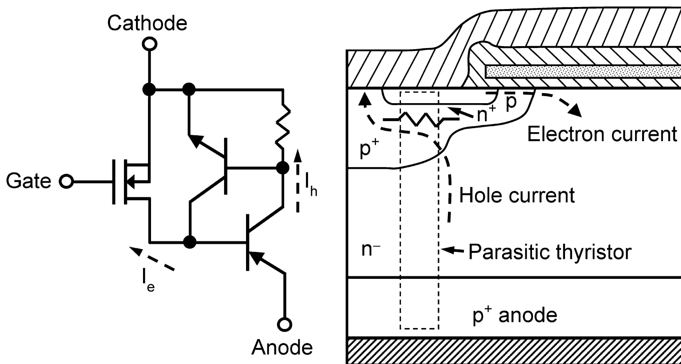

Fig. 5.7. The parasitic thyristor in IGBT structure.

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When the conduction current increases, both electron and the hole components increase with a similar trend, although not the same proportion due to the moderate variation of α_{PNP} current gain as a function of the current. The voltage across the p-base/n$^+$-emitter junction is approximately equal to the voltage drop at the p-base under the n$^+$-emitter layer, and can be expressed as

$$V_{\mathrm{p/n+}} = R_{\mathrm{p}} I_{\mathrm{h}} = R_{\mathrm{p}} \alpha_{\mathrm{PNP}} I_{\mathrm{f}}. \tag{5.18}$$

To activate the n–p–n transistor, the voltage across the top junction needs to be effectively forward-biased, i.e. $V_{\mathrm{p/n+}} \geq 0.7\,\mathrm{V}$. Therefore, the upper limit of steady-state current before latch-up point can be calculated by using Eq. (5.18) as

$$I_{\mathrm{f,SL}} = \frac{0.7}{R_{\mathrm{p}} \alpha_{\mathrm{PNP}}} = \frac{0.7}{\rho_{\mathrm{p}} \frac{L_{\mathrm{E}}}{W d_{\mathrm{p}}} \alpha_{\mathrm{PNP}}}, \tag{5.19}$$

where ρ_{p} is the resistivity of the p-base as a function of the doping concentration of the region, L_{E} is the n$^+$-emitter length, W is the device width in the paper direction, and d_{p} is the p-base depth under the n$^+$-emitter. Figure 5.8 gives a detailed schematic to highlight these parameters. It is understood that Eq. (5.19) is an approximate equation with the assumption that the whole hole current will flow through the p-base region underneath the n$^+$-emitter. In reality, there is certain percentage of the hole current which does not flow underneath the n$^+$-emitter.

During the initial stage of turn-off process, the electron current diminishes to zero after the MOS channel is removed. However, the hole current remains unchanged, and still flowing through the p-base region to bias the upper junction. Then, it will be a reasonable assumption to say that the n–p–n transistor gain remains similar at the beginning of the turn-off process. But, this shall not be treated as an absolute assurance of safe device operation from latch-up. The

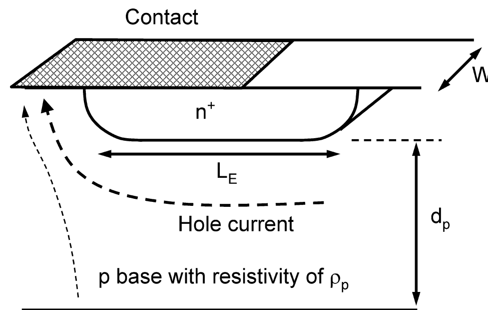

Fig. 5.8. Dimensions for the calculation of p-base resistance.

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reason is, because the p–n–p transistor gain changes from its on-state value to a higher value during the turn-off transition. Equation (5.10) indicates that the p–n–p transistor gain is a function of the undepleted base width, L_B. During on-state, the base width, L_B, is almost the same as the n^--drift region length $2d$, and it stays at the same value for various current levels. During turn-off, the IGBT device sustains part of the supply voltage at and after the initial stage of the period. The high voltage depletes the drift region and shortens the effective base width of the p–n–p transistor. Considering the change in n-drift region width for the symmetrical IGBT device, Eq. (5.10) can now be re-written as

$$\alpha_{\mathrm{PNP,DY}} = \frac{1}{\cosh\left(\frac{2d-\sqrt{\frac{2\varepsilon_{\mathrm{s}} V_{\mathrm{DY}}}{qN_{\mathrm{d}}}}}{L_{\mathrm{a}}}\right)}, \tag{5.20}$$

where V_{DY} is the voltage across the IGBT during the turn-off dynamic, N_d is the drift region doping, and ε_s is the silicon dielectric constant. For the case of asymmetrical structure, the undepleted base width is approximately equal to the n-buffer width. The transient voltage across the device raises the p–n–p transistor gain and this makes the latch-up limit lower and the device more liable to be latched up. In a sense, when an IGBT device operates below the latch-up current limit during steady-state does not imply that it can be turned off successfully. The ratio of static latch-up current limit versus the dynamic one can be derived as

$$\frac{I_{\mathrm{f,SL}}}{I_{\mathrm{f,DL}}} = \frac{1-\alpha_{\mathrm{PNP,SL}}}{1-\alpha_{\mathrm{PNP,DL}}} = \frac{1-\frac{1}{\cosh\left(\frac{2d}{L_{\mathrm{a}}}\right)}}{1-\frac{1}{\cosh\left(\frac{2d-\sqrt{\frac{2\varepsilon_{\mathrm{s}} V_{\mathrm{DL}}}{qN_{\mathrm{d}}}}}{L_{\mathrm{a}}}\right)}} \approx \frac{1-2e^{-\frac{2d}{L_{\mathrm{a}}}}}{1-2e^{-\frac{2d-\sqrt{\frac{2\varepsilon_{\mathrm{s}} V_{\mathrm{DL}}}{qN_{\mathrm{d}}}}}{L_{\mathrm{a}}}}}, \tag{5.21}$$

where V_{DL} is the voltage across the IGBT device at the dynamic latch-up during turn-off. For the inductive load, the voltage overshoot during turn-off is larger than that of the resistive load. It is then expected to have a lower dynamic latch-up current limit. To reduce the inductive overshoot, a gate resistor can be used to adjust the rate of MOS channel turn-off and this will vary the rate of current change at the initial stage of turn-off, i.e. the electron current component. This has a greater influence on the voltage overshoot and therefore on the dynamic latch-up current limit.

Various effects were made to bring up the latch-up current limit, such as introduction of deep p^+ diffusion under the n^+-emitter, adjusting the n^+-emitter length (Baliga *et al.*, 1984), lifetime reduction in the n-base region

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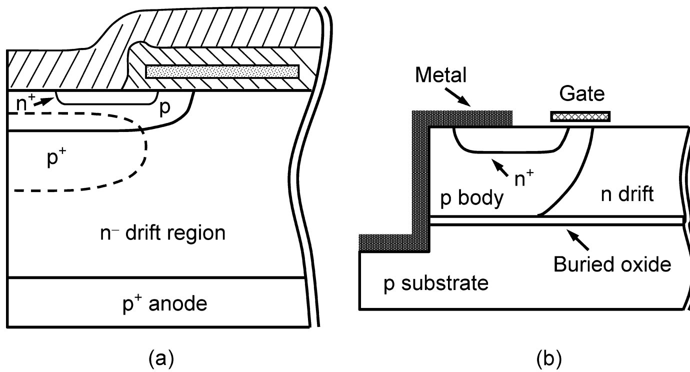

Fig. 5.9. (a) The p^+ implantation under the emitter on episubstrate and (b) the trench metal structure on SOI substrate.

(Chang *et al.*, 1983; Goodman *et al.*, 1983), retrograde p-well and dual p-well implantation for lateral IGBT structure (Disney and Plummer, 1993), self-aligned trenched cathode contact (Nezar and Mok, 1993), and formation of metal sinker to the substrate (Liang *et al.*, 1999). Among them, the p^+ sinker layer on vertical structure, as shown in Fig. 5.9(a), is commonly used to reduce the p-base resistance under the n^+-emitter to lower the upper n–p–n transistor gain. On SOI substrate, the trenched metal sinker, as shown in Fig. 5.9(b), is a good candidate to raise the latch-up limit and to relieve the thermal stress caused by the buried oxide layer.

5.5. Temperature Effects

Temperature variations pose an important role in the IGBT performance. Key features, such as the forward conduction voltage, turn-off time, and latch-up current level are all affected (Baliga, 1987). The MOS channel region has a positive temperature coefficient, but the bipolar junction has a negative temperature coefficient. This makes the on-state voltage coefficient of an IGBT device, $V_{ce(on)}$, at low current region to be negative, e.g. more like a p–i–n diode. And at medium current region, the conduction voltage varies less than that of the MOSFET device as the device temperature increases. At high-current region, the channel resistance will dominate the on-state behavior, and the temperature coefficient on forward voltage becomes more positive.

The IGBT turn-off time is dominant by the open-base transistor tail time made by the recombination process. When temperature goes higher, the

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minority carrier lifetime is found to be higher and the recombination process takes a longer time to complete. Higher temperature also makes the p–n–p transistor current gain to be higher and subsequently the hole/electron current composition becomes higher as well. A higher percentage of hole current compounds the lifetime effect and makes the bipolar current tail time even longer.

High temperature creates the negative effect on the latch-up current level as well. Basically, both transistor gains increase with temperature and so the p-base resistance. The p-base resistance is influenced by the variations of the intrinsic carrier concentration and the carrier mobility when temperature varies. A higher temperature will raise the intrinsic concentration and lower the carrier mobility. The amount of variation is a function of the background doping concentration. For a medium-high doping region, the increment on the intrinsic concentration plays less dominant role compared to the effect on reduction in carrier mobility. Overall, the p-base resistance becomes higher at a higher temperature. All three variations make the structure more liable to be latched up.

5.6. Series and Parallel Operations

Connecting IGBT devices in series allows high-power/high-voltage semiconductor switches to be realized. In series operation, the current flowing through each IGBT is the same but the anode-to-cathode voltage of each of the IGBTs may be different due to inherent differences in the device parameters. Because of the differences in both device parameters and gate-drive circuits, a control for voltage balancing needed for each device to endure an equal magnitude of anode-to-cathode voltage in the transient and steady-state operations, e.g. an active gate-drive balancing technique for series-connected IGBTs was reported (Gerster, 1994). For this technique, a closed-loop control is integrated in each gate drive circuit to adjust the anode-to-cathode voltage of each of the series-connected IGBTs to an equal value.

Paralleling of IGBT devices helps to reduce conduction losses and thermal stress (Dapkus, 1994). It should be noted that parallel configuration to take advantage of the lower price of smaller devices should not be attempted without due consideration of technical and gate-drive complexity. In general, all IGBTs are operating at the linear region, i.e. at low-voltage conduction. Hence, the two key device parameters, *I–V* slope and starting knee voltage, decide the current sharing under steady-state conduction. However, during transient operations,

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the current balancing becomes more complicated than simply matching these two key parameters. Other parameters, such as the gate threshold voltage, the input and output capacitances, the stray inductance in each leg, and even the amount of excess charge storage in the drift region become equally important during transient operations.

When two or more IGBT devices are parallel-connected, the anode-to-cathode voltage across each device is hard-wired to be the same during steady state. Thus, for a given load current, one IGBT will carry a higher or lower proportion of current than other mismatched ones if the gate voltage is not properly adjusted. As long as the device current remains below the maximum specified limit on the data sheet, the current imbalance is initially not critically important. However, the device that carries more and more current may exceed the rated junction temperature of about 150° C if the heat sink design does not take the current imbalance into consideration. One factor that can reduce current imbalance is by identifying and matching the temperature coefficients (Baliga, 1985) of IGBT devices used in parallel. Experimental results (Yang and Liang, 1996) show that incremental current variation, $\Delta I_{A,IGBT}/\Delta I_{LOAD}$ (the change in IGBT current versus the change of total load current) of each IGBT depends on the operating current level. This means, an IGBT shares the least portion of current at low-current level may eventually share the highest portion of current at the high-current level. This makes the uncontrolled current matching more difficult. That is, by matching the current sharing at one current level does not guarantee the equal sharing at another current level. A good gate control is thus needed to ensure equal current sharing at all current levels (e.g. Tabata *et al.*, 1998) by *di/dt* control and with closed-loop balancing controller (Hofer *et al.*, 1996).

5.7. Device Operations under Soft-switching

The use of soft-switching inverters in industry has good potential since it allows the effective utilization of faster device switching speed for higher switching frequency at lower loss, lower *dv/dt* for low EMI (electromagnetic interference), and handling of higher power density. Soft-switching operations are formed in zero voltage or zero current conditions by adding additional components in the circuit. Figure 5.10 shows the circuit and the current–voltage waveforms associated with the zero-voltage (ZV) conditions. Under soft-switched conditions, the IGBT produces a voltage spike and a current bump during switching transitions. The phenomena are mainly due to the lag of conductivity modulation in the drift region during turn-on, and the ineffective removal of stored charge in the same region during turn-off. The phenomena have been observed and

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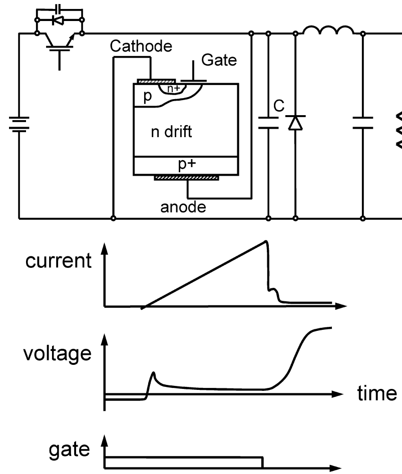

Fig. 5.10. IGBT device under zero-voltage switching and the voltage and current waveforms.

analyzed as mentioned in various publications (Kurnia *et al.*, 1992; Widjaja *et al.*, 1994, 1995).

During zero-voltage transition, prior to the current flow into the IGBT anode, a negative voltage of about -1 V clamped by the reverse-conducting diode is applied across the device. The gate signal is applied prior to the current to become forward conduction. Although technically the IGBT device has been turn-on, there is so far no current flowing through the device. When the in-rush current flows through the IGBT device, similar to a p–i–n diode, the forward recovery phenomenon occurs in the lightly doped drift region. As such, the dynamic voltage spike occurs at the initial period of the zero-voltage switching. The spike disappears when the voltage across the n-drift region drops to its normal steady-state value at full conductivity modulation. During turn-off period, the anode voltage increases rather slowly due to the snubber capacitor C in parallel. Without a strong depletion field, the excess carriers in the transistor base region cannot be removed effectively at the initial period. They were swept away by the increased electric field later on when the depletion junction gradually builds up. The final outcome gives a current bump at the tail of the current waveform. Figure 5.11 shows the experimental waveforms of a commercial IGBT under zero-voltage soft-switching conditions.

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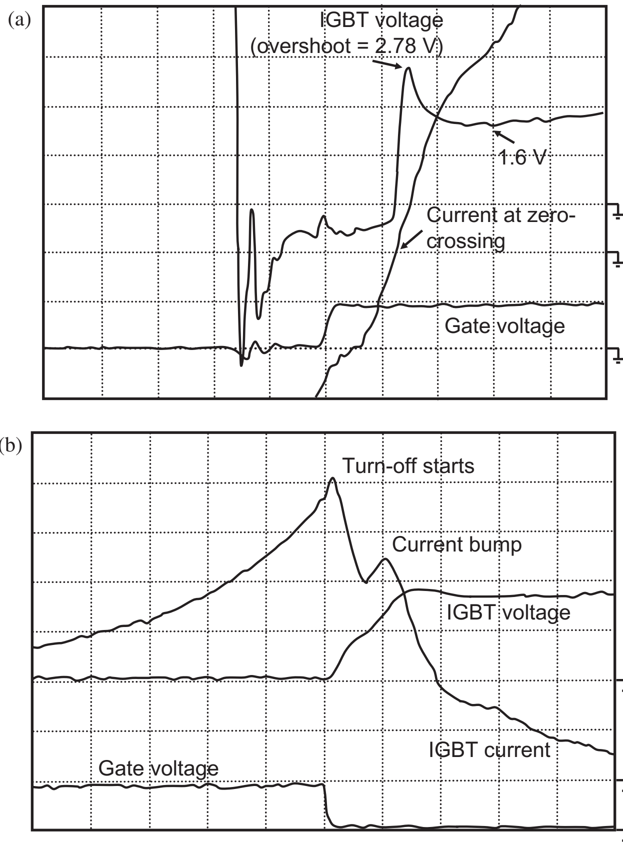

Fig. 5.11. (a) Measured forward voltage spike during turn on: time base (1 μs/div), gate voltage (20 V/div), IGBT current (2 A/div), and IGBT voltage (1 V/div). (b) Measured current bump during turn off: time base (1 μs/div), gate voltage (20 V/div), IGBT current (1 A/div), and IGBT voltage (20 V/div).

5.7.1. Dual-Gate IGBT for ZV Soft-Switching

The dual-gate bidirectional IGBT as shown in Fig. 5.12 can improve the situation by applying suitable gate signal to the second gate (Yuan, 1999). Prior to the current flow into the IGBT for zero-voltage turn-on transition, the auxiliary gate is turned on for some period of time. A small portion of the diode current will be diverted to flow through the IGBT in the reverse direction. Thus, the hole carriers will be injected from the upper p^+-emitter into the bulk drift region for recombination with the electron carriers flowing through the

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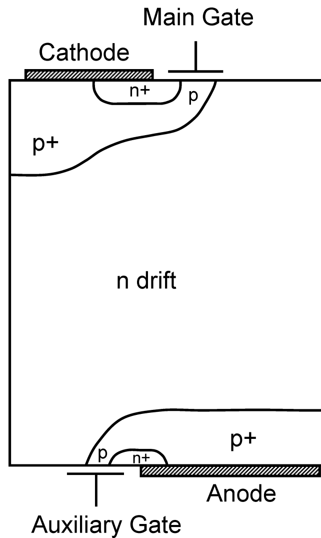

Fig. 5.12. Dual-gate IGBT device for soft-switching applications.

channel along the auxiliary gate. Then, the resistance of drift region will be dramatically reduced by the existence of hole–electron carriers prior to forward conduction. The relief on the "conductivity modulation lag" reduces the formation of forward voltage spike during turn-on transition. Figure 5.13 gives the simulation data for different *dJ/dt* conditions for both ordinary IGBT (forward current density of 225 $\mathrm{A/cm^2}$) and the dual-gate IGBT (for the same forward current density and the reverse current density of 16 $\mathrm{A/cm^2}$). The results show that, under fast transient condition, the forward voltage spike can be reduced by up to 60%.

Under the zero-voltage turn-off transition, the anode voltage increases rather slowly due to the snubber capacitor across the IGBT device. By switching on the auxiliary gate, the inversion layer is formed to short the junction J1 so as to reduce the hole injection into the drift region during the turn-off period. The accumulation of excess hole carriers can be greatly relieved. As a result, a shorter turn-off time can be achieved. Simulation results are shown in Fig. 5.14. When the ordinary IGBT turns off with snubber capacitor, a current bump occurs as expected after the MOS-channel was cut off. It is found that, without lifetime control ($\tau_{\mathrm{HL}} = 2.18\,\mu\mathrm{s}$), the dual-gate structure has a better performance than that of the ordinary structure with lifetime control ($\tau_{\mathrm{HL}} = 0.95\,\mu\mathrm{s}$).

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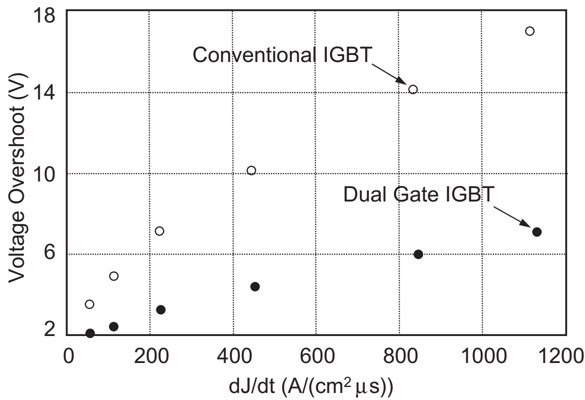

Fig. 5.13. Simulated forward voltage overshoots for the conventional and dual-gate IGBTs of the same drift region.

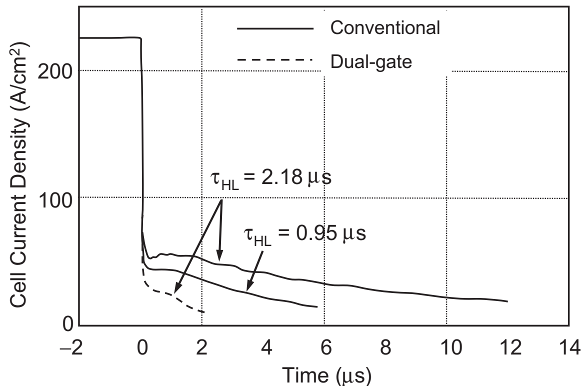

Fig. 5.14. Simulated turn off times for conventional and dual-gate IGBTs of the same drift region.

5.8. Lateral IGBT Structure

Much interest in development is focused on the integrated power modules using (Bi)CMOS and DMOS process technologies. The integration feature requires the power IGBT structure to be formed in the lateral way, so that other circuit devices can also be fabricated on the same substrate. The basic lateral IGBT structure on p bulk substrate is shown in Fig. 5.15, which consists of

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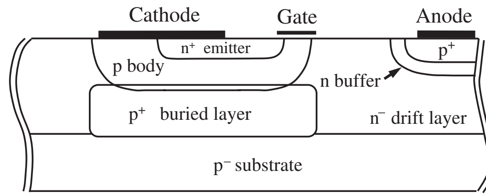

Fig. 5.15. Lateral IGBT structure on p-substrate.

a gate channel region, p–n–p vertical bipolar transistor, and a p–n–p lateral bipolar transistor. The majority of the anode current flows laterally through the n-drift region in parallel with the p-substrate to arrive at the channel/p-body region then to cathode contact. Some of the anode current flows in the substrate and may be collected by the substrate contact or other part of the circuit elements. The n-buffer layer next to the anode p^+-emitter is placed to raise the breakdown voltage as similar to that of the punch-through vertical structure. The p^+ buried layer creates a low-resistance path between the p-body and the p-substrate. This increases the current conductivity from the substrate to the body region and thus increases the lateral current ratio.

The lateral current ratio is defined as the lateral current collected by the cathode versus the anode current. When the IGBT is fabricated on the SOI wafer, the lateral current ratio is then 100%. A good lateral IGBT device is said to achieve a high lateral current ratio, proper forward and reverse breakdown voltages, a low on-state conduction voltage, and the turn-off time below a few hundred nanoseconds. Liang and Hor (1995) showed the variations of parameters on drift region length, drift region doping, buffer layer doping, and inclusion of buried layer to the influence on device performance. On bulk wafer, the lateral current ratio can be increased by including the buried layer and shortening the drift region length. The forward breakdown voltage is affected by the drift region concentration as similar to that of the vertical structure. The reverse breakdown voltage occurs at the buffer region and affected by its concentration and length. The turn-off time is a function of drift region concentration, drift region length, and buffer layer concentration. By including a large buried layer, higher drift layer doping, shorter drift layer length, and higher buffer layer doping will shorten the turn-off time. However, a higher buffer layer concentration will cause a higher on-state voltage drop. Similar to the vertical IGBT structure, lifetime control can also be made in the n^--drift region near the n-buffer to speed up the turn-off transient.

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5.9. Integrated Current Sensor

A current sensor in power electronic circuits is usually needed in two aspects, namely to provide the precise current information for feedback control (Chow *et al.*, 1992; Manduteanu, 1993; Shen *et al.*, 1994; Liang and Hor 1995; Lang *et al.*, 1998), and otherwise to provide critical overcurrent information for protection purpose (Seki *et al.*, 1994; Robb *et al.*, 1994; Shimizu *et al.*, 1994). For the latter, the sensing ratio on overcurrent protection can be much coarse compared to the former one which needs to be kept almost constant at all current levels. In some cases, due to MOS-channel saturation at the high-current region, the IGBT anode voltage can be used to represent the overcurrent information for protection purpose (Luo *et al.*, 2000). The advantage of having an integrated current sensor on the same die is to provide the direct sensing information with less parasitic involved in comparison to the usage of external current sensors, not to mention that the external sensing circuits can be complex and bulky. Preferably, the integrated sensor is fabricated together during the process of IGBT fabrication.

The accurate current sensor suitable for smart power integration in the lateral insulated-gate bipolar transistor (LIGBT) structure is described in this section. The same sensor structure can also be applied for other types of MOS-controlled bipolar structures. For MOS-bipolar devices, the electron and hole current components need to be sensed individually in order to precisely predict the amount of device current at all operating current levels. The rationale, in brief here, is that the electron/hole current composite ratio, i.e. electron current versus hole current, does not keep to a constant level when the device current level varies. Other more stringent requirements for a constant sensing ratio are on the temperature variations and in transient operation.

The integrated sensor should not affect the normal operation of power devices. This requires the current taken by the sensor to be very small compared to the main device current. Besides, the sensing current should be maintained possibly at a constant ratio with minimum variation in respect to the main current under large load variations, e.g. during both the steady-state and transient operations, gate voltage variations, and over the range of operating temperature.

The basic principle in the design of a sensor is simple and it requires a parallel current path. Using the principle of the parallel resistors shown in Fig. 5.16, the sensor current can be made to be a small and fixed ratio to the main current by properly controlling the resistive ratio between R_s and R_m.

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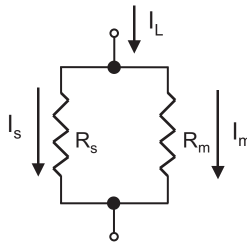

Fig. 5.16. Parallel resistive current paths.

Therefore, the sensing ratio will be $I_s/I_o = R_m/(R_s + R_m)$. By putting the value of R_s to be much greater than that of R_m, the sensing ratio can be made to be very small.

A sensor structure was designed (Liang *et al.*, 1998) to enable sensing of the electron current together with the hole current in the correct proportion. In this structure, two additional regions and contacts are added to the standard LIGBT structure at the cathode area. The device has the cathode split into two contacts with one sensor contact inserted in between. The device structure is shown in Fig. 5.17 and its peak doping levels, junction/profile depths, and contact positions are given in Table 5.1. The anode and n-buffer layers are not shown in the figure since the main focus is on the sensor structure in the cathode area.

The electron current sensor layer (sensor-1 contact) and the hole current sensor layer (sensor-2 contact) are routed and electrically connected together. The doping concentration of the n sensor layer can be determined through process and device simulations, such that the electron current sensing ratio is of

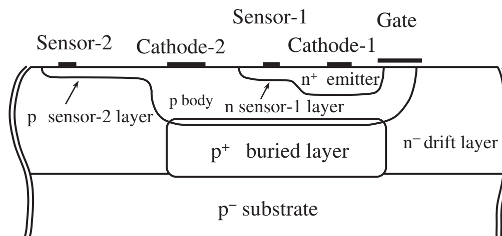

Fig. 5.17. Electron and hole current sensors integrated in the lateral IGBT structure (anode and n-buffer are not shown).

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Table 5.1. LIGBT (with current sensor) layer dimensions and doping profiles.

Layer	Lateral dimension (μm)	Peak doping concentration (cm^{-3})	Depth (μm)
n^+-emitter	6.0	1×10^{20}	1.0
p-body	15.2	1×10^{18}	5.0
p^+ buried	12.0	2×10^{18}	Between 8.0 and 12.0
n^--drift	45.0	1×10^{15}	10.0
p^+ anode	5.0	2×10^{19}	2.0
n-buffer	7.0	4×10^{16}	5.0
p^- substrate	—	2×10^{14}	40.0
p sensor	7.3	2×10^{15}	1.0
n sensor	3.5	5×10^{18}	1.5

the same proportion as the hole sensing ratio. This criterion is a very important and is the prerequisite to ensure the constant sensing ratio over the whole range of current and gate voltage variations. The two cathode contacts are also routed together. Both the cathode and the sensor contacts are grounded externally. Referring to Fig. 5.17, it must be noted that the position and length of cathode-1 contact are important factors in ensuring sufficient potential difference within the n^+ layer between cathode-1 and sensor-1 contacts. This potential difference, typically about a few hundred millivolts, would result in some electron current flowing into the sensor-1 contact.

The design gives a good performance in sensing ratio when the cathode current and gate voltage are varied. However, it suffers by a large variation in sensing ratio when the operating temperature varies. For the doping levels in Table 5.1, the electron sensing ratio varies in a range of as large as $\pm 40\%$ between 250 and 450 K. For the hole sensing ratio, it varies in a smaller scale of $\pm 9\%$. This makes the variation on the overall sensing current to be rather large.

Here, the physics behind the variation and the solution to remedy the problem will be described. Intuitively, the variation in sensing ratio is caused by the variation in (parallel) resistance ratio. And, there are two main factors that cause the resistance ratio variation with temperature, namely the modulation of carrier mobility and the change of intrinsic carrier concentration. These two factors jointly, but not equally, affect the semiconductor resistivity of the

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conduction paths taken by the electron and hole currents. Thus, the sensor ratio varies. These two factors have opposite temperature dependency, interacting to minimize the spread of the sensor ratio variation. The hole current sensing ratio was found to be relatively more constant as the counteracting becomes more effective. However, the situation was not so for electron current sensing ratio.

The carrier mobility in the cathode region is a function of doping concentration, types of dopants, and temperature as described in (Masetti *et al.*, 1983). Although the magnitude of variation is a function of the dopant concentration, the general trend is that the mobility drops when the temperature increases. Therefore, the higher the temperature is, the higher the resistivity will be. The second factor is on the intrinsic carrier concentration. When the temperature rises, the intrinsic carrier concentration will go up. This phenomenon will counteract the mobility degradation to lower the resistivity. However, this phenomenon is less obvious in the n^+-emitter/sensor region due to the high background doping concentration. It is more obvious in the p-body/sensor region for the reason of lower doping concentration. This explains the situation well on why the hole current sensing ratio has less variation with temperature compared to the electron current sensing ratio.

An innovative approach to solve this problem of sensing ratio variation was found through analyzing the current flow pattern of electron carriers. And, the approach of having the “flat-top” doping profile in the n^+-emitter region is introduced to minimize the difference in doping concentration between the paths taken by the sensor and cathode currents. When looking at the distribution of doping concentration along vertical cut from wafer surface to the substrate, as shown in Fig. 5.18, the “flat-top” profile gives a constant doping concentration till certain depth and then starts to fall off. This approach replaces the original Gaussian doping profile associated with a typical diffusion process. In comparison, the profile now has a more uniform doping concentration for the entire cathode region and a steep transition in doping concentration at the internal junction. Therefore, the cathode current and the sensor current would flow over a region of the same doping concentration. The result on applying this technique gives a significant improvement in the variation of the electron current ratio against temperature variation as the resistivity of the main current path will vary at the same manner as that of the sensor current path. With this approach, the variation of the total sensing ratio against temperature can be reduced to about $\pm 9\%$ between 250 and 450 K, as obtained by the analysis results.

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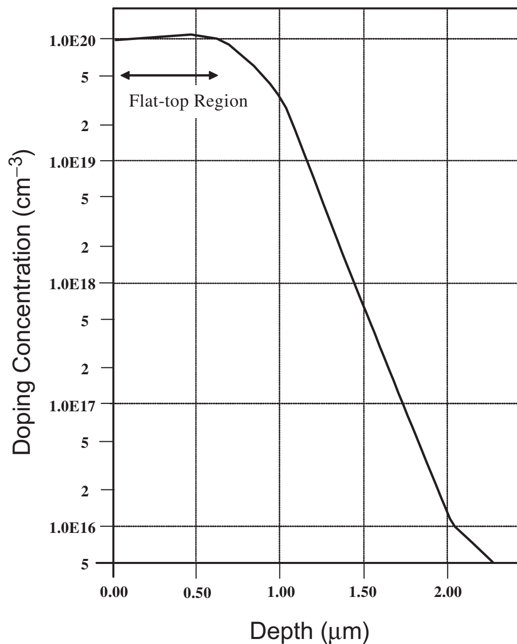

Fig. 5.18. The doping profile along the vertical cut showing the flat-top portion.

5.9.1. Fabrication Aspects

The numerical results indicate a clear need for a flat-top profile at n^+-cathode region to reduce the variation of the electron current ratio against temperature. To create the flat-top profile, a double-implantation, single-anneal method is needed. For both the first and second implantation, the dosage of phosphorus impurity implanted into the silicon is similar. They differ only in the acceleration energy with which the impurity ions are injected into the silicon wafer. Adjustments should be made to produce a set of implantation energies that will create a flat-top doping profile.

However, after the double-implantation single-anneal process, it was found to have the persistent dip of concentration profile at the surface of the n^+-emitter region although the rest of the region whose concentration beneath the surface is flat. Therefore, an oxidation step was added after the annealing and drive-in step to rectify this problem. The doping impurity (initially present in the silicon) redistributes at the interface due to the segregation effect (Sze, 1985) to lift n^+ concentration up and remove the dip near the surface. The flat-top

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profile of the n^+-emitter region is shown in Fig. 5.18 from the process simulator by applying the above steps at cathode region. As to the sensor region, by choosing a shallower doping profile, process simulation shows that it was possible to obtain a good flat top profile using just a single-implantation process.

Detailed fabrication process steps are described here. The process started with p-type substrate with ⟨100⟩ wafer of uniform doping of $2 \times 10^{14}\,\text{cm}^{-3}$. The p-type buried layer was formed by Boron implant with energy 200 keV and dose $8 \times 10^{14}\,\text{cm}^{-2}$ followed by a 10 minutes post-implant anneal in nitrogen ambient at 1000°C. Then a 5 μm epitaxial-layer was grown with phosphorus doping of $1 \times 10^{15}\,\text{cm}^{-3}$. This layer basically forms the low-doped n-drift layer. The p-body region was then formed by boron implant with energy 200 keV and dose $7 \times 10^{14}\,\text{cm}^{-2}$ followed by a 300 minutes post-implant anneal/drive-in in nitrogen ambient at 1050°C. The n-buffer region was then formed by phosphorus implant with energy 100 keV and dose $2 \times 10^{14}\,\text{cm}^{-2}$ followed by a 220 minutes post-implant anneal/drive-in in nitrogen ambient at 1050°C. The p-anode region was then formed by boron implant with energy 50 keV and dose $3 \times 10^{15}\,\text{cm}^{-2}$ followed by a 10 minutes post-implant anneal in nitrogen ambient at 1000° C. The p-sensor region was then formed by boron implant with energy 120 keV and dose $2 \times 10^{11}\,\text{cm}^{-2}$ followed by a 120 minutes post-implant anneal/drive-in in nitrogen ambient at 1000° C. Afterwards the gate oxide is grown in dry oxygen ambient for 20 minutes at 1000° C. Finally, a double implanted n^+-emitter and shallow n-sensor regions were formed followed by metallization and passivation. Figure 5.19 shows the simulated process profiles which were created by the series of process steps discussed here.

5.9.2. Performances

The wafer micrograph in Fig. 5.20 shows the fabricated lateral IGBT and the integrated sensor contact positions. The dc performance was tested with various anode bias, gate bias, and device temperature. A special heating platform was set up to maintain the wafer at a predefined elevated temperature. Measurements were made for the linear region (function as a power switch) as well as the saturation region (function as an amplifier).

5.9.2.1. *DC Measurement in the Linear Operating Region (Switch Operation)*

Figure 5.21 shows the measured values of sensing ratio over a range of temperatures with anode current values between 250 and 600 mA per cell group.

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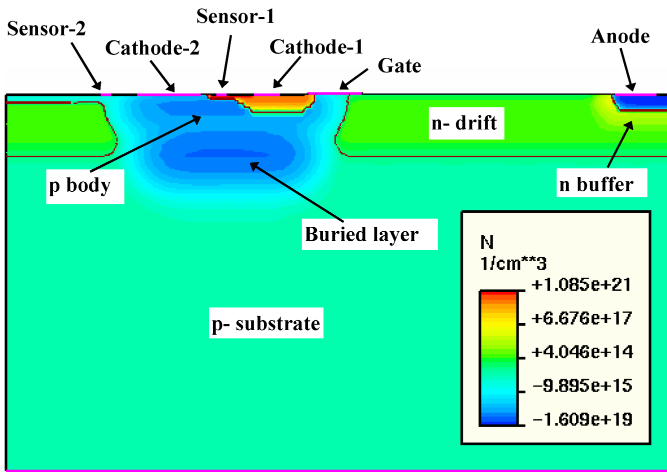

Fig. 5.19. Device profile obtained by process simulation.

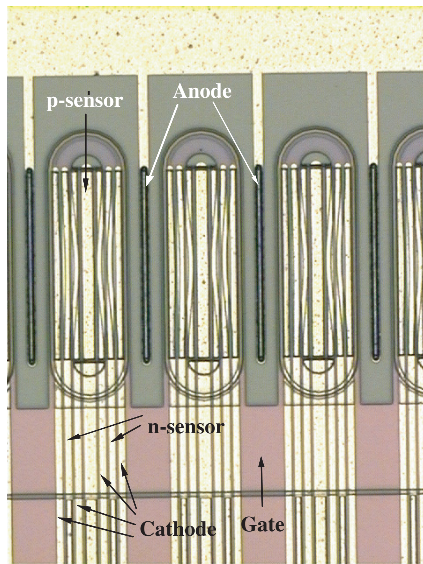

Fig. 5.20. The micrography of a fabricated lateral IGBT with integrated current sensor.

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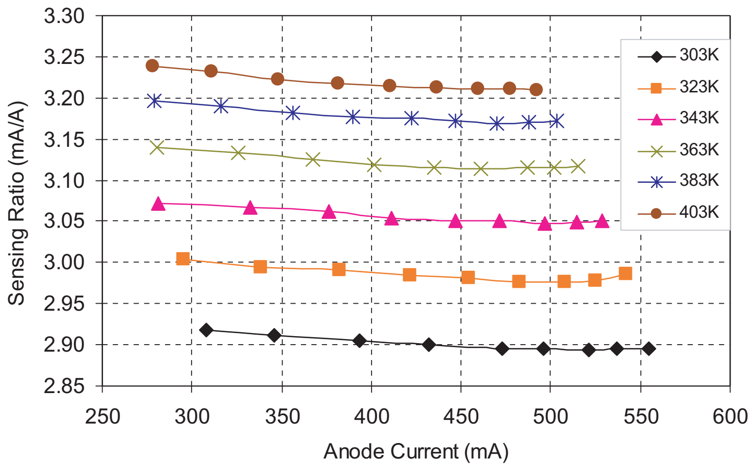

Fig. 5.21. Variations of current sensing ratio against anode current at various temperatures (under linear operating mode, as a switch) with a constant gate bias.

The curves show that the sensor current ratio remains fairly constant with the anode current density and has a stronger dependence on the temperature variations. It is observed that the sensing ratio becomes less dependent on temperature variation at a higher temperature. A total variation of around ±5.2% from the average sensing ratio is observed when the device is at temperature range between 303 and 403 K.

The gate bias sensitivity on the current sensing ratio is shown in Fig. 5.22. The values of sensor ratio change in a peak-to-peak range from 1.96% to 2.41% (or within ±1.21%) with the gate voltage. The sensing ratio changes by ±5.22% for temperature from 303 to 403 K as seen. A similar characteristic is observed that the temperature variation dominates the current ratio variation and the effect becomes weaker toward the higher temperature region.

5.9.2.2. *DC Measurement in the Saturation Operating Region*

Similar dc tests were conducted with the device operating in the saturation region (as an amplifier device). The device operating in saturation region conducts a higher current and at a higher anode voltage compared to the linear region. The device then has a higher loss, and therefore, a higher thermal stress.

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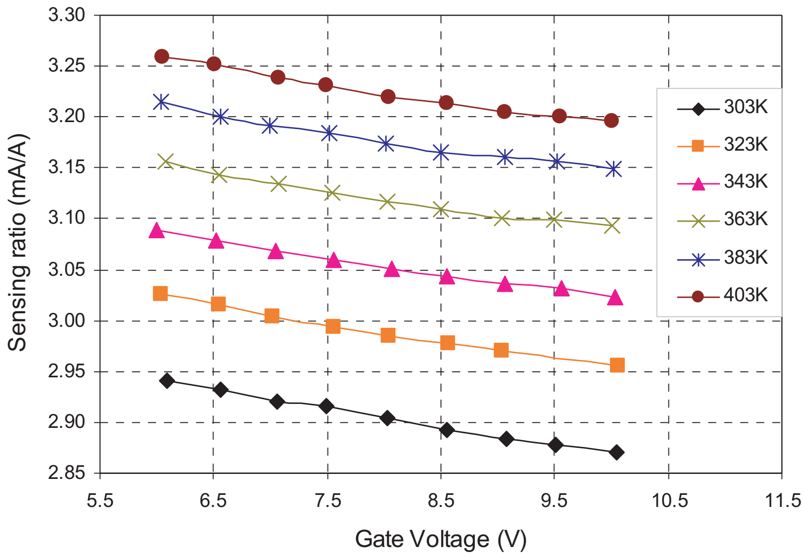

Fig. 5.22. Variations of current sensing ratio against gate voltage at various temperatures (linear operating region, as a switch) with a constant anode current.

Furthermore, the current increases with the high temperature under the same electrical biasing condition. When the compound current was sufficiently large, the thyristor latch-up effect was triggered.

The measurement results for ramping anode voltage are plotted in Fig. 5.23, while the results for ramping gate voltage measurement are plotted in Fig. 5.24. Similar to the case of linear region, the temperature effect dominates the current sensing ratio variation. The total sensing ratio varies within ±0.85% with respect to the anode current variation, and within ±1.73% with respect to the gate voltage variation.

5.9.2.3. *Transient Response*

Transient response was observed during the switching of the lateral device from on-state to off-state. The waveforms are shown in Fig. 5.25. The turn-off time, measured from 100% to 10% of the load current is around 20 μs. The sensor ratio tracks the transient responses quite well.

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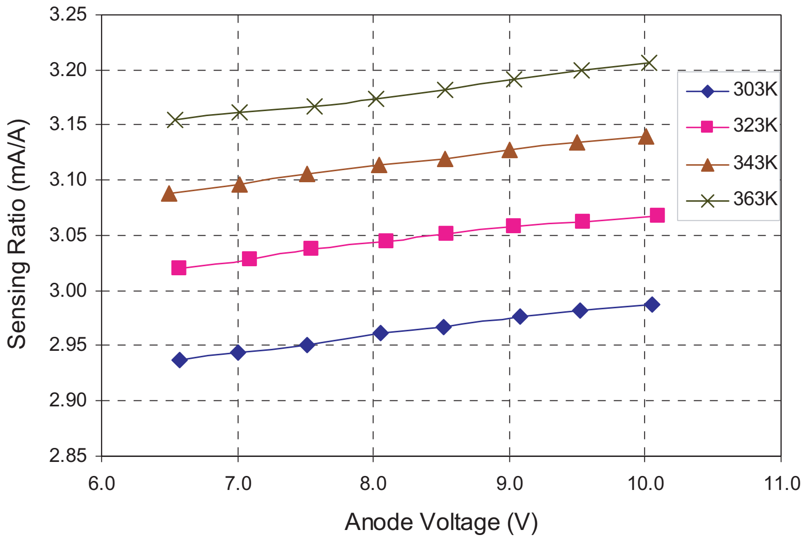

Fig. 5.23. Variations of current sensing ratio against anode voltage at various temperatures (saturation operating region, as an amplifier device).

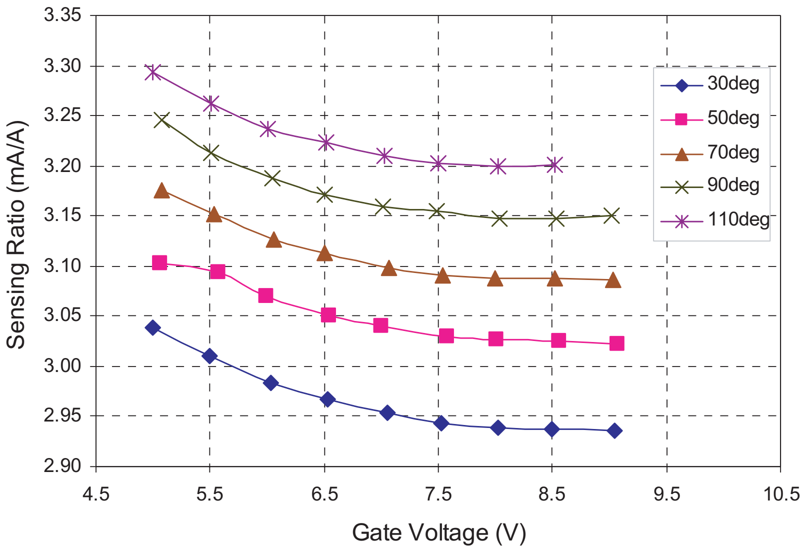

Fig. 5.24. Variations of current sensing ratio against gate voltage at various temperatures (saturation operating region, as amplifier device).

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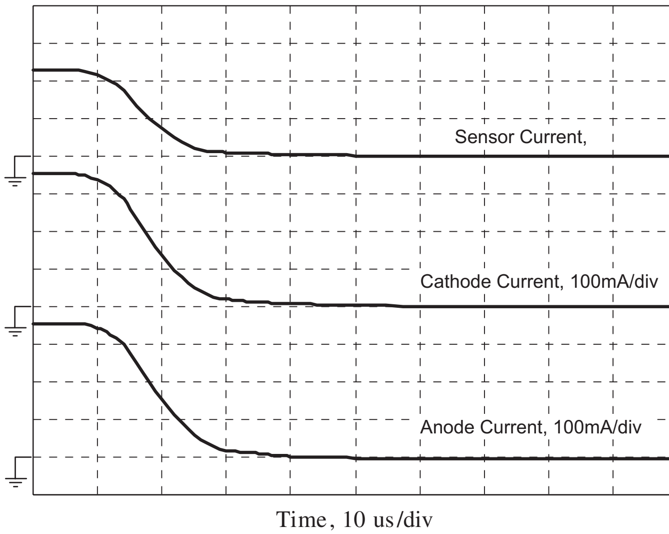

Fig. 5.25. Transient response waveforms during device turn off.

5.10. Safe Operating Area

The safe operating area (SOA) is an important aspect for operations in steady-state conduction, blocking, and switching. The shape of SOA for an IGBT is similar to that of a typical power MOSFET and is shown in Fig. 5.26. The corner shape of the safe operating area depends on device switching speed. For

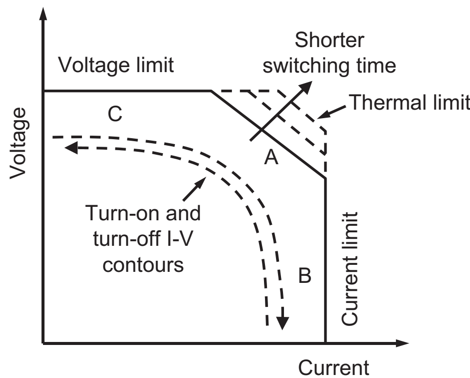

Fig. 5.26. The device SOA region.

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different switching speeds, the forward operating area is thermally limited and the SOA varies as shown by the boundary line A. This is the boundary where both the anode current and voltage are simultaneously large, i.e. the high thermal stress region. Boundary line B is limited by the maximum allowable anode current of the IGBT which is below the latch-up limit. This limit is usually reached at higher gate voltage and especially at high operating temperature. Boundary line C is set by the maximum anode-to-cathode breakdown voltage of the IGBT. The voltage is determined by the open-base p–n–p transistor, i.e. BV_{CBO}. Practically, the SOA of an IGBT is more robust than that of the power MOSFET.

5.11. Overcurrent Protection

The overcurrent protection scheme is usually necessary to built a part of the function in power integrated circuits. The protection scheme needs to distinguish different types of fault conditions, e.g. moderate over-load or sever short-circuit, and to react accordingly based on the device SOA limit. At the same time, the protection circuit should be concise and suitable for integration. The behaviors of the IGBT device under various fault conditions were studied in the literature and useful protection schemes were proposed (Biswas *et al.*, 1991; Chokhawala *et al.*, 1995; Valentine, 1995). The protection in practice should cover a wide range of overcurrent condition. Under moderate overload, the device current is higher than its continuous current rating (I_{CCR}) but remains below the maximum pulse current level (I_{MPC}). The failure mechanism for IGBT device under the moderate overload is thermal runaway. Under the short-circuit condition, the current is much larger and usually exceeds the I_{MPC} rating. Under such a high current, the IGBT device needs to be turned off immediately or less than a few microseconds to avoid fatal destruction.

Usually, a time-delay control is implemented for overcurrent protection to avoid unnecessary shutdown caused by transient current surges. In practice, it ranges from a few microseconds for the catastrophic fault to a few milliseconds for the moderate overload condition. The variation of delay time is a nonlinear function of load current as shown in Fig. 5.27. The delay-time limit is derived from the device SOA. In general, it covers four major zones, namely the thermal limitation, the maximum rating on pulsed current, the short-circuit withstanding capability, and the maximum current level limited by the transistor gain (I_{MAX}). At room temperature, the boundary on thermal limitation at certain current level is determined by the time taken to reach 450 K junction temperature under single-pulse and normal-gate voltage condition. Depends on the gate voltage, the maximum short-circuit current level varies (Shen, 1996).

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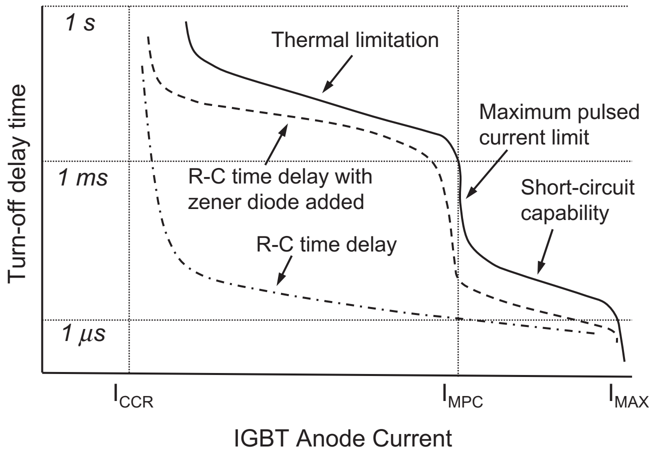

Fig. 5.27. The turn-off delay time under different overcurrent conditions.

A resistor–capacitor first-order circuit can be used and to be charged by the anode voltage to serve as a simple timer for turn-off delay time. The voltage across the capacitor can be expressed as

$$V_C = KI_A(1 - e^{-\frac{t}{RC}}), \tag{5.22}$$

where R and C are the resistance and capacitance and K is the conversion gain factor between the anode voltage and anode current, i.e. $KI_A = V_A$. Under overload condition, the IGBT device works in its saturation region, e.g. at high voltage and high current. The value K can approximately be assumed as a constant. If a voltage V_p is set as the reference voltage for the shutdown threshold, that is, when V_C is equal or higher than V_p, then the IGBT gate drive will be removed. The delay time can be found as

$$t_{to-turn-off} = RC \ln \frac{KI_A}{KI_A - V_p}. \tag{5.23}$$

The curve of time delay using simple R–C timer is shown in Fig. 5.27. It can be seen that, although the delay time is controlled within the SOA transient limit, it has a far distance away from the actual thermal limitation boundary. This is because the time constant needs to be kept small to meet the critical limit on short-circuit withstanding limit. In this case, the allowable overload capability of the device is not fully utilized. One way to make the full use of the SOA transient limit is to insert a zener diode in parallel with the resistor to provide a voltage-dependent two-stage time constant. This is shown by

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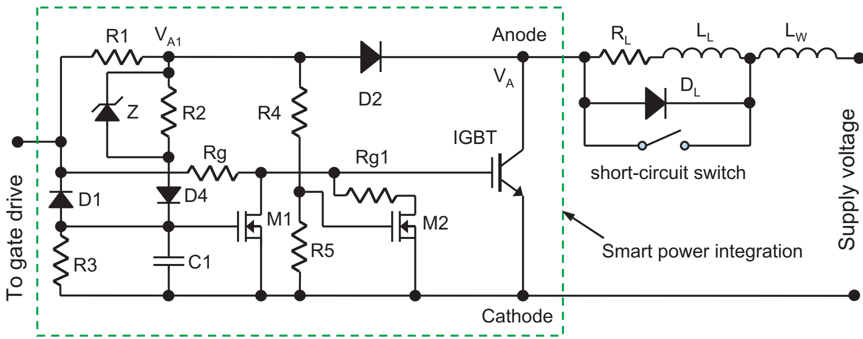

Fig. 5.28. Overcurrent protection circuit.

(Z // R2) and C1 in the circuit of Fig. 5.28. When the anode voltage, which is approximately proportional to the anode current, goes up and the voltage across R2 goes above the zener diode breakdown voltage, V_Z, the zener diode breaks down and the capacitor C1 will be charged up at a much smaller time constant. This is because the zener diode has a smaller dynamic resistance after breakdown. The delay time can now be expressed as:

$$t_{\text{to-turn-off}} = \begin{cases} (R_Z//R_2//R_3)C_1 \ln\left(\dfrac{KI_A - V_Z}{KI_A - V_Z - V_p}\right) & \text{for } I_A > I_{MPC}; \\ (R_2//R_3)C_1 \ln\left(\dfrac{KI_A}{KI_A - V_p}\right) & \text{for } I_{MPC} > I_A > I_{CCR}; \\ \text{Infinitive} & \text{for } I_{CCR} > I_A. \end{cases} \quad (5.24)$$

The curve with zener diode added is also shown in Fig. 5.27 which has a closer match to the profile of SOA transient boundary.

For new generation IGBTs, they have a higher I_A/V_g gain for high conductivity and low anode voltage drop. But, they also have a lower short-circuit withstanding time (Otsuki *et al.*, 1993; Seki, 1994; Iwamuro *et al.*, 1995). The short-circuit withstanding time is typically below 5 μs. Although the delay time can be made very short by reducing the value of capacitance C1 to a minimum, in practice, it may suffer from parasitics and noise interference. Therefore, it would not be a reliable configuration for the R–C network to provide a delay time in the sub-microsecond zone. Also, the delay time should be relatively longer than the switching transition time to ensure its normal operation. One solution to prolong the allowable time before turn-off is to lower the gate

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voltage as the short-circuit withstanding capability is also related to the gate voltage.

The protection circuit in Fig. 5.28 has incorporate the feature to lower the gate voltage when a direct short-circuit occurs. When this happens, the voltage across the IGBT goes nearly the same level as the supply voltage. The diode D2 provides the isolation and keeps voltage V_{A1} to a constant level which is related to the magnitude of gate drive voltage. Resistors R4 and R5 divide the voltage and turn the MOSFET M2 on. When M2 is turned on, it pulls Rg1 to ground and lowers the voltage to the IGBT gate contact. A lower gate bias will then prolong the short-circuit withstanding capability. At the same time, capacitor C1 keeps being charged up via zener diode and R2. When the capacitor voltage reaches the threshold value V_p, MOSFET M1 turns on and the IGBT gate contact is grounded. The device is now turned off.

The operation can be quantitatively analyzed. Under the normal operating condition, the anode voltage is low and diode D2 is at its on-state. The voltage V_{A1} is

$$V_{A1} = V_A + V_{D2}, \tag{5.25}$$

$$V_{C1} = \frac{R_3}{R_2 + R_3}(V_{A1} - V_{D4}) < V_{th,M1}, \tag{5.26}$$

where V_{D2} is the voltage across diode D2, V_{D4} is the voltage across diode D4, $V_{th,M1}$ is the threshold voltage to turn on MOSFET M1. When overcurrent occurs, V_A will increase and this brings V_{A1} to be higher as well. As a result, capacitor C1 is charged to a higher voltage. The time constant is

$$\tau_1 = (R_2//R_3)C_1 = \frac{R_2 R_3}{R_2 + R_3}C_1. \tag{5.27}$$

When V_{C1} reaches the threshold voltage $V_{th,M1}$, M1 turns on to pull down the voltage to the gate contact. The IGBT is then turned off.

A zener diode is used to distinguish between the moderate overload and the catastrophic conditions. When V_A rises above $V_Z + V_{th,M1}$, the device will be regarded as in the short-circuit operation, and the turn-off delay time must be shortened within its withstanding capability. The time constant is now

$$\tau_2 = (R_z//R_2//R_3)C_1 \approx R_z C_1, \tag{5.28}$$

which is much lower than τ_1. As mentioned, M2, R4, R5, and Rg1 are added to provide the current-limiting feature by reducing the voltage to the gate contact

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to prolong the short-circuit withstanding time. When the short-circuit occurs, diode D2 is turned off, and the voltage to the gate contact of MOSFET M2 is

$$V_{\text{gate,M2}} = \frac{R_5}{R_1 + R_4 + R_5} V_{\text{gate-drive-input}} \geq V_{\text{th,M2}}, \tag{5.29}$$

where $V_{\text{th,M2}}$ is the threshold voltage of MOSFET M2. As the IGBT gate voltage is reduced, the fault current can be limited to a lower value. The response time for the current-limiting effect to appear is determined by the time constant of

$$\tau_3 = \frac{(R_1 + R_4)R_5}{R_1 + R_4 + R_5} C_{\text{g,M2}}, \tag{5.30}$$

where $C_{\text{g,M2}}$ is the gate input capacitance of MOSFET M2. This time constant is normally very short and below 1 μs. While the short-circuit withstanding capability is extended, the time delay circuit (with zener diode breakdown) functions concurrently to turn off the gate voltage to IGBT in the similar manner as described earlier, but with a more comfortable delay-time period. The turn-off delay-time is described as shown in Eq. (5.24). Figure 5.29 shows the measured circuit performance to protect an IGBT rated around 15 A. Based on the SOA limit at gate voltage of 15 V, the time constant of τ_1 is set to be 7ms and τ_2 is set to be 16 μs. The triangular data point is measured at a reduced gate voltage when the protection circuit lowers it from 15 to 10 V to prolong the short-circuit withstanding capability.

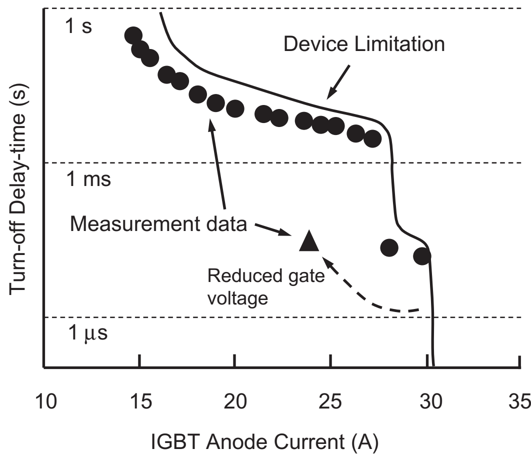

Fig. 5.29. Measured turn-off delay time of the protection circuit of Fig. 5.25.

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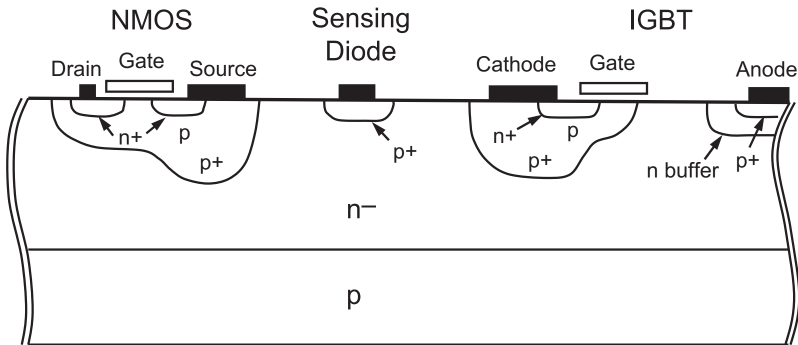

Fig. 5.30. Integration of key components for the overcurrent protection circuit on bulk substrate.

The protection circuit can be fabricated together with the IGBT device to form the smart-power integration on the same silicon die, e.g. Fig. 5.30 showing the integration of key components and Fig. 5.31 showing part of the silicon die. The chip was fabricated with a total of eight masks on a single-side $n^-(5 \times 10^{14}\ cm^{-3})\langle 100 \rangle$ epi-wafer with zener diode as an external component. Resistors are not shown and they can be formed by polysilicon deposition. Short-circuit faults have been applied to verify the effectiveness of the proposed

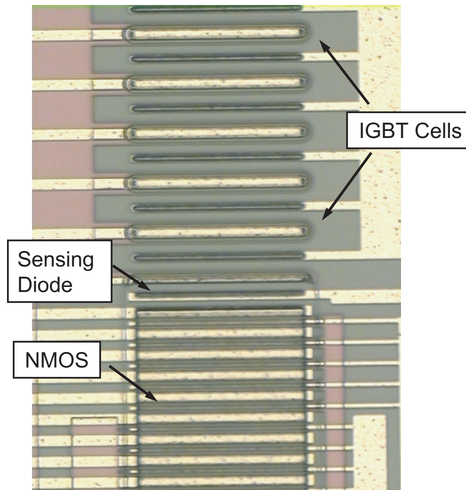

Fig. 5.31. Micrography of key components of the overcurrent protection integrated circuit.

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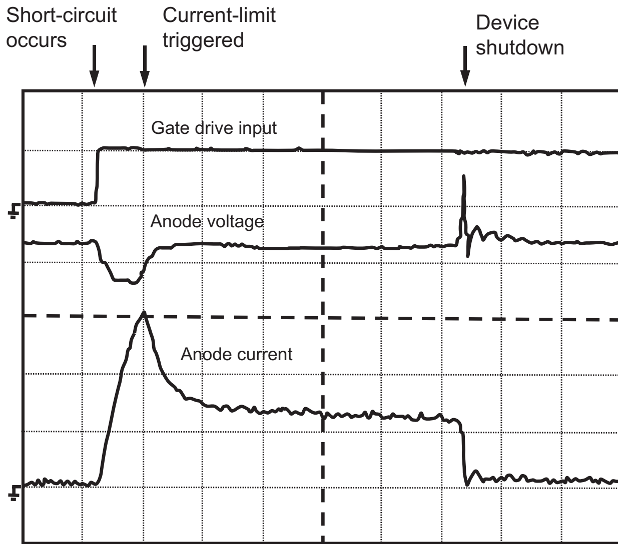

Fig. 5.32. Measured hard-switch fault (at 105 V supply voltage, 800 A/cm^2 anode current density); time scale: 2 μs/div; anode voltage scale: 25 V/div; anode current scale: 2 A/div.

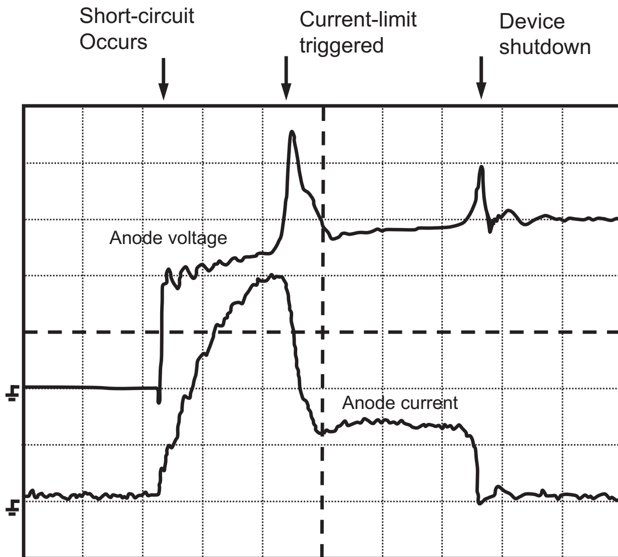

Fig. 5.33. Measured fault under load (at 105 V supply voltage, 1068 A/cm^2 anode current density); time scale: 1 μs/div; anode voltage scale 35 V/div; anode current scale: 2 A/div.

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protection scheme. Two types of short-circuit faults, namely the "hard switch fault" and the "fault under load", can occur during the operation of power electronic circuits. The "hard switch fault" condition is described as that the short-circuit fault exists before the IGBT is turned on, that is, the IGBT will be turned on under short-circuit condition. The "fault under load" condition is described as that the short-circuit fault occurs during the normal IGBT conduction state.

Figure 5.32 shows the measured waveforms of anode voltage and current of hard switched fault (at 800 A/cm^2) at supply voltage of 105 V and gate voltage of 10 V. The device recovers from the fault by shutting down the gate drive after about 10 μs. Another short-circuit fault under load (at 1060 A/cm^2), as shown in Fig. 5.33, is applied to the device, and similar recovery is made after about 5 μs.

5.12. Vertical IGBT Fabrication Process

To fabricate a vertical IGBT device, it follows the following basic steps (Chang, 1995; Luo *et al.*, 2000) as shown in the table below.

Step	Process	Recipe
1	Starting wafer: n^-/p^+ epi-wafer ⟨100⟩ drift region concentration and thickness determined by the breakdown voltage specification	Wafer cleaning
2	Field oxidation for 4000 Å	Dry–wet–dry oxidation 1100°C, 10 min (dry), 25 min (wet), 5 min (dry)
3	Photolithography, p-well mask	
4	Field oxide etching	Buffered oxide etching (BOE)
5	p-well implant: BF_2	80–100 keV, 5E15/cm^2
6	Photoresist strip	
7	p-well drive-in and oxidation	1050°C, 60–70 min (wet)
8	Photolithography, active area mask	

(*Continued*)

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Step	Process	Recipe
9	Oxide etching	BOE
10	Photoresist strip	
11	Gate oxidation	900°C, 30–60 min (dry)
12	Polysilicon deposition (LPCVD)	650°C, 5000 Å
13	Oxide deposition (APCVD)	
14	Photolithography, polygate mask	
15	APCVD oxide etching	
16	Polysilicon etching	HNO_3: CH_3COOH: HF
17	Gate oxide and APCVD oxide etching	BOE
18	p-body (channel region) implant: B	35–40 keV, 1E14/cm^2, 7°
19	p-body drive-in and oxidation	900°C, 20 min (dry O_2)1100°C, 180 min, N_2
20	Oxide removal	
21	n^+ cathode implant: As	80 keV, 5E15/cm^2
22	n^+ cathode drive-in	900°C, 30 min (dry O_2)950°C, 30 min, N_2
23	Oxide removal	
24	PCVD oxide and BPSG densification	1.5 K SiO_2–7.5 K BPSG 900°C, 30 min
25	Photolithography, contact mask	
26	Contact opening	BOE
27	Photoresist strip	
28	Al deposition, 1.5–2 μm	400°C, 30 min
29	Photolithography, metal mask	
30	Al etching	
31	Sintering	

The corresponding device profiles are shown in Fig. 5.34 by process simulation.

5.13. Related MOS-Bipolar Structures

5.13.1. Emitter Switched Thyristor (EST)

The emitter switched thyristor was designed to have a lower on-state voltage drop and a higher voltage–current saturation capability. The device structure

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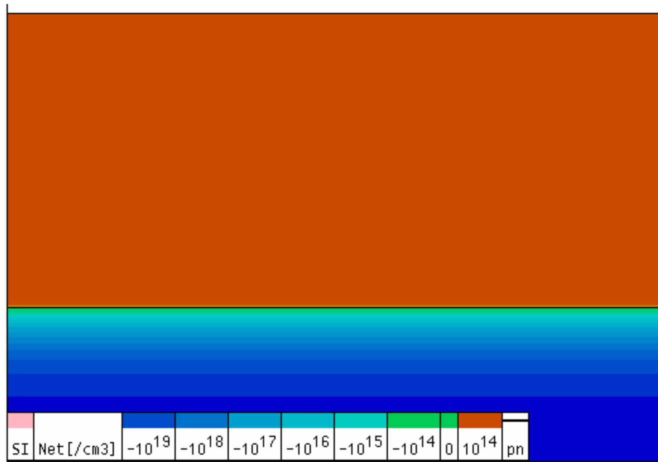
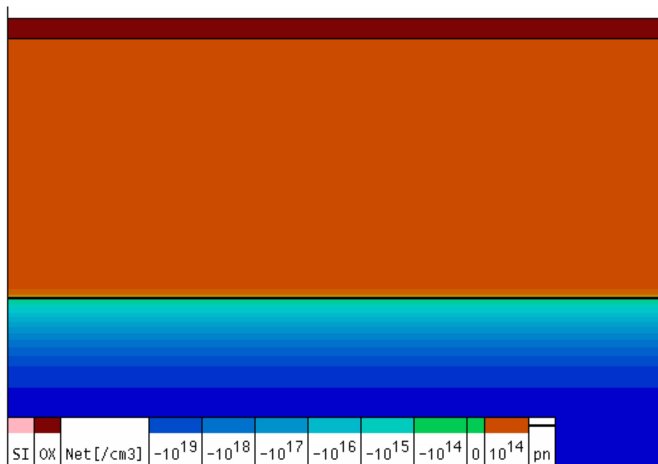


(a) Starting wafer.



(b) Wafer cleaning and field oxidation.

Fig. 5.34. IGBT process details by simulation.

evolved from the conventional EST (Shekar, 1991a; Bhalla and Chow, 1994), the dual-channel EST (Shekar, 1991b), and to the recent dual-gate EST (Sridhar and Baliga, 1996). The device operation is initially similar to that of the IGBT, however, due to the latch-up of the main parasitic thyristor and dual-gate operation, it has a good on-state voltage–current capability and

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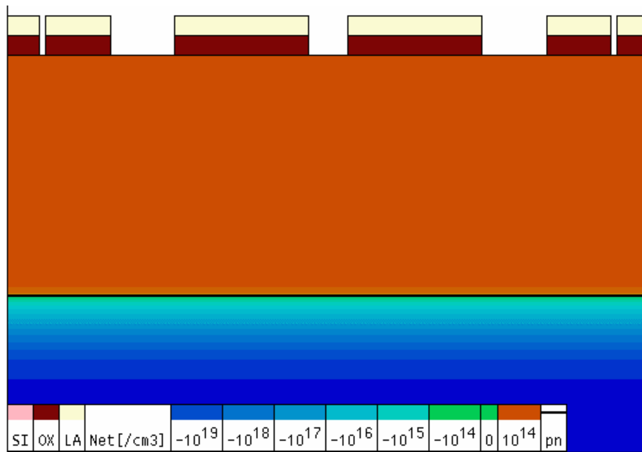
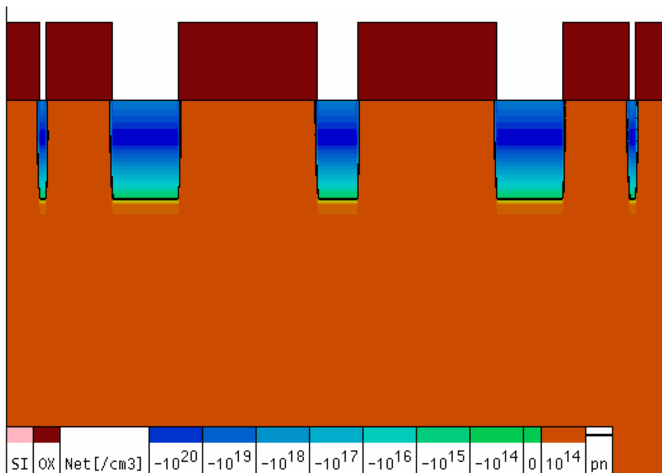


(c) P.R. coating, p+ well mask, and field oxide etch.



(d) p+ well implant and P.R. strip.

Fig. 5.34. (*Continued*)

higher saturation capability. The device structure is shown in Fig. 5.35. In the structure, two MOS gates, namely Gates 1 and 2, are used to form the inversion channels for conduction. During the operation, Gate 2 can be turned off to switch the operation mode from dual-gate operation to dual-channel conduction (Sridhar and Baliga, 1996), if desired.

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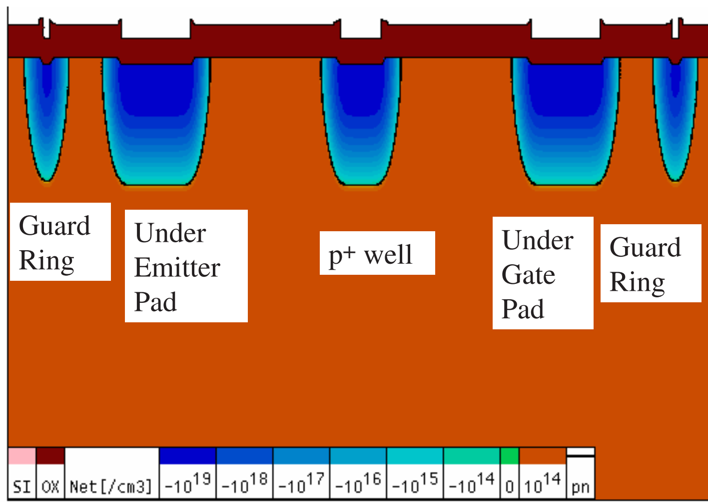
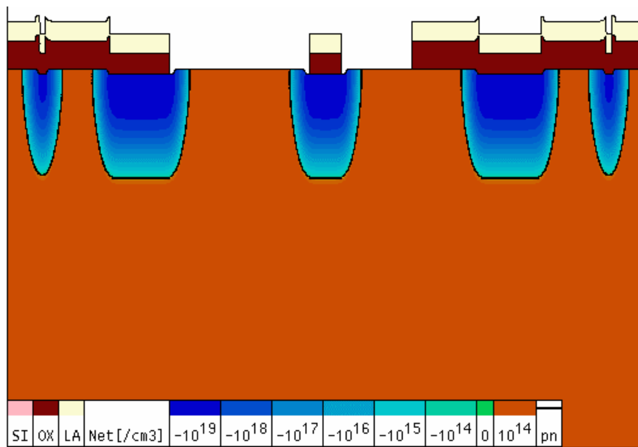


(e) p⁺ well drive-in.



(f) P.R. coating, active area mask, and oxide etch.

Fig. 5.34. (*Continued*)

When both gates are applied a positive voltage, the device functions like an IGBT, however with multiple conduction paths due to two cathode contacts. From cathodes, electron carriers flow through the MOS channels to arrive at the n^--drift region. And from anode, hole carriers flow into the drift region for conductivity modulation and also partially through the p-base region forming

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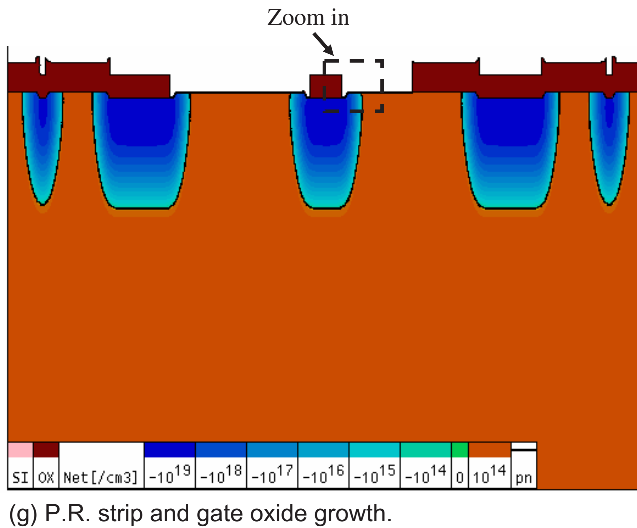
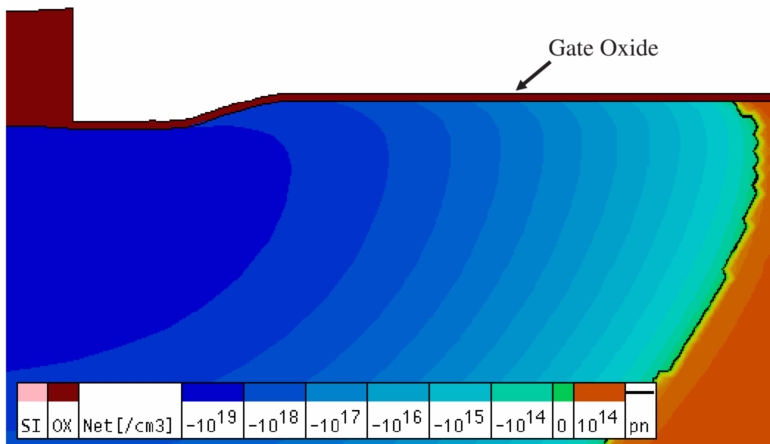


(g) P.R. strip and gate oxide growth.



(h) P.R. strip and gate oxide growth.

Fig. 5.34. (*Continued*)

the transistor current. The main thyristor latch-up occurs when the current goes to a higher level and the p-base/n$^+$-junction becomes forward-biased. Now, the device enters the EST region with a large part of current supply through the main thyristor. The on-state voltage reduces to be as low as about

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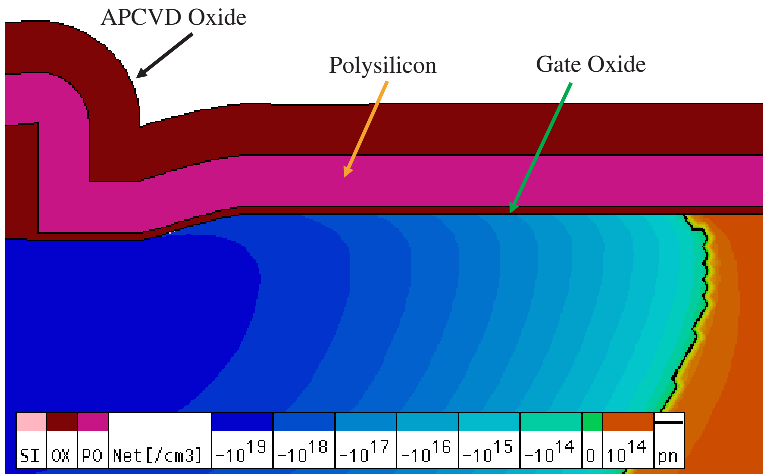
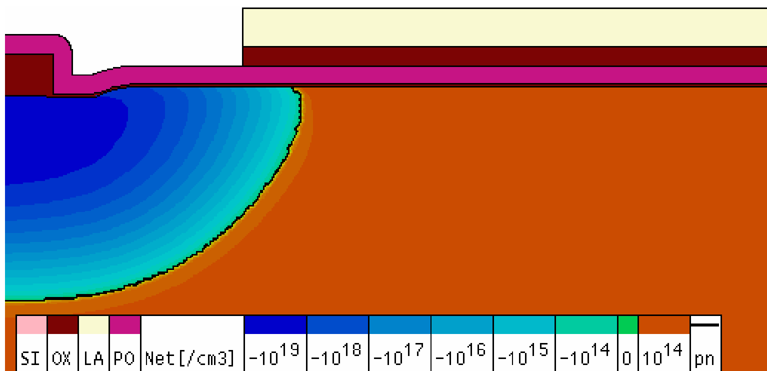
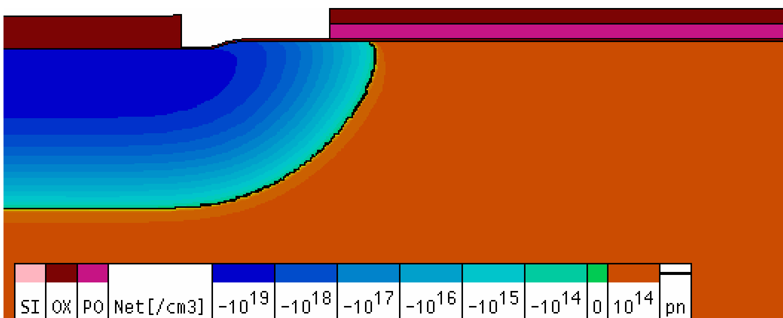


(i) Polysilicon deposition and APCVD oxide deposition.



(j) P.R. coating, poly mask, and APCVD oxide etch.



(k) P.R. strip and poly etch.

Fig. 5.34. (*Continued*)

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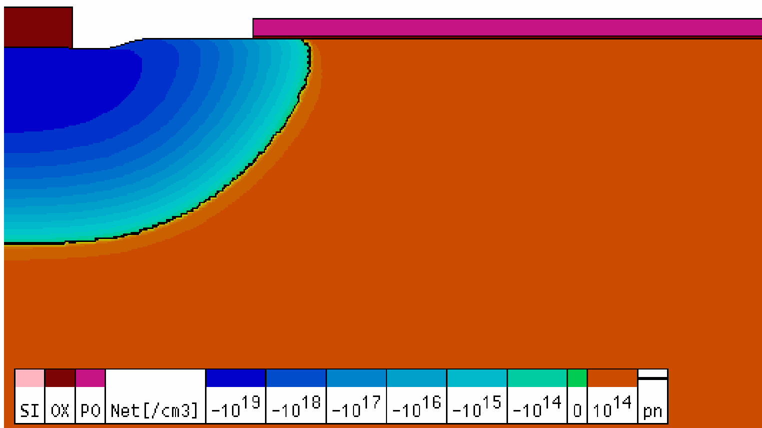
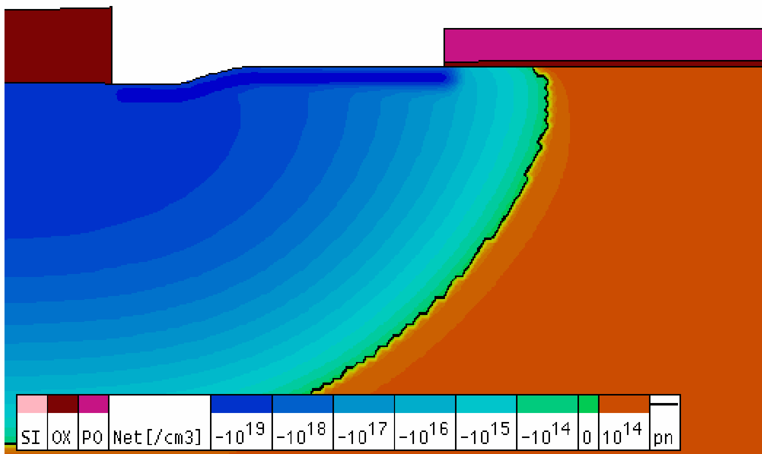


(l) Gate oxide and APCVD oxide etch.



(m) p-Base implantation.

Fig. 5.34. (*Continued*)

1.1 V at high current conduction. The thyristor current is partitioned and flows through both MOS channels. The voltage rating of the forward safe operation area is now limited by the breakdown voltage of the short-channel lateral MOSFET under Gate 2. If the bias at Gate 2 is turned off, the device can operate at a higher saturation voltage as that of the dual-channel EST. The structure has two p^+ regions to divert the hole current to two cathodes. At

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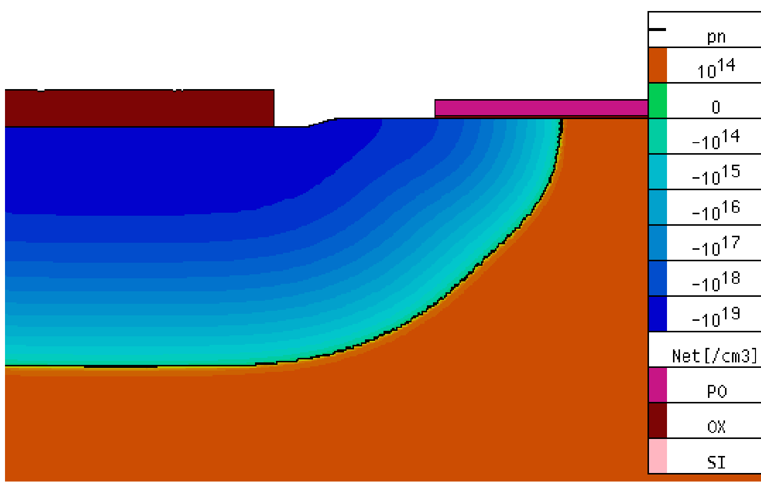
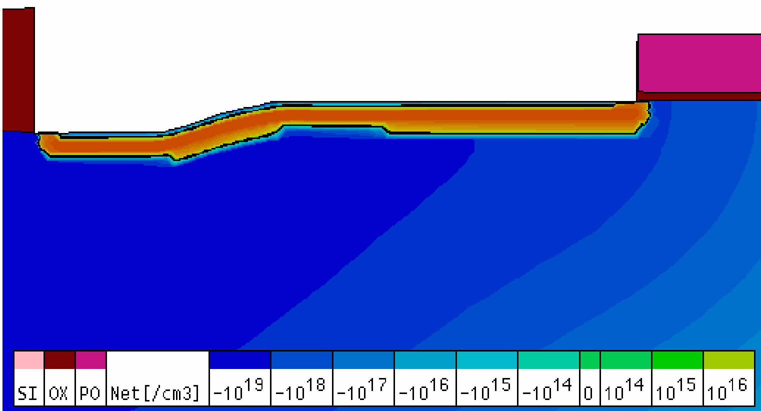


(n) p-Base drive-in.



(o) Remove thin oxide and n⁺ implant.

Fig. 5.34. (*Continued*)

a very high current density, the gate control is lost due to the latch-up of the parasitic thyristors. As reported in Sridhar and Baliga (1996), the normal operation region is around 800 A/cm^2 with the parasitic thyristor latch-up current density at above 1000 A/cm^2. Figure 5.36 gives the *I–V* curves of high voltage, e.g. 600 V, MOSFET, IGBT, and the dual-gate EST devices for a brief on-state comparison. For the modern third generation IGBT, devices, the forward

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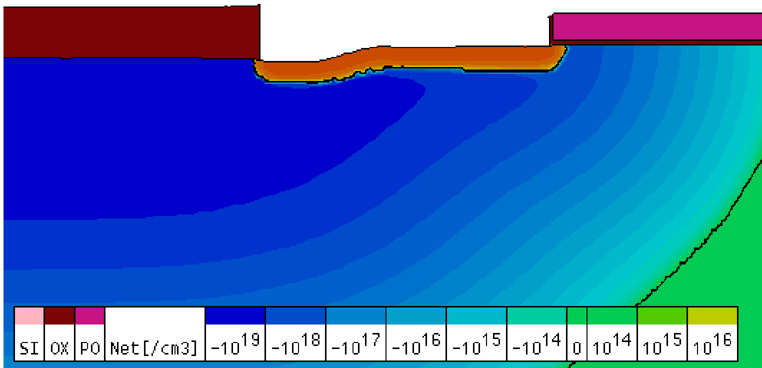
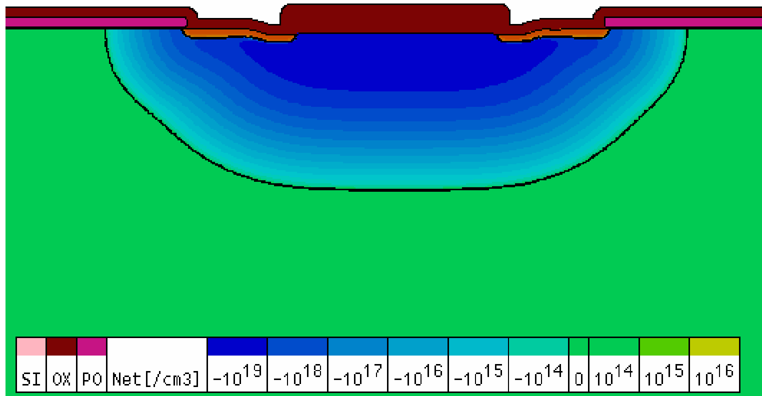


(p) n+ drive-in.



(q) Remove thin oxide and APCVD oxide deposition.

Fig. 5.34. (*Continued*)

voltage drop at 100 A/cm^2 ranges from 1.3 to 1.7 V, which is still higher than that of EST at around 1.1 V drop.

5.13.2. Base-Resistance-Controlled Thyristor (BRT)

The structure of the asymmetric dual-gate BRT is shown in Fig. 5.37 (Kurlagunda and Baliga, 1995) which evolved from the earlier structure of BRT by Nandakumar *et al.* (1991). The structure utilizes the MOS gate control

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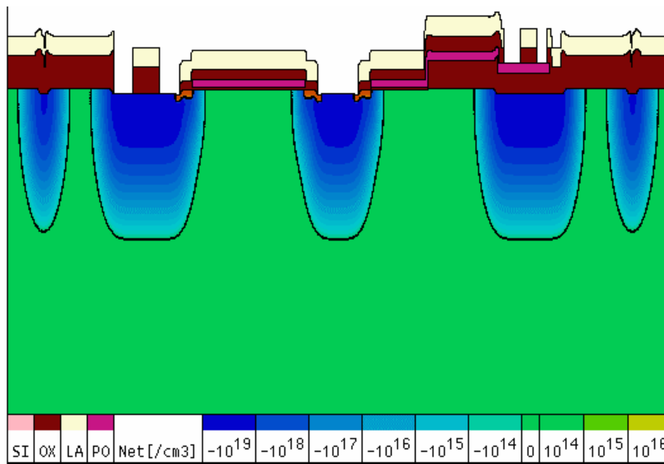
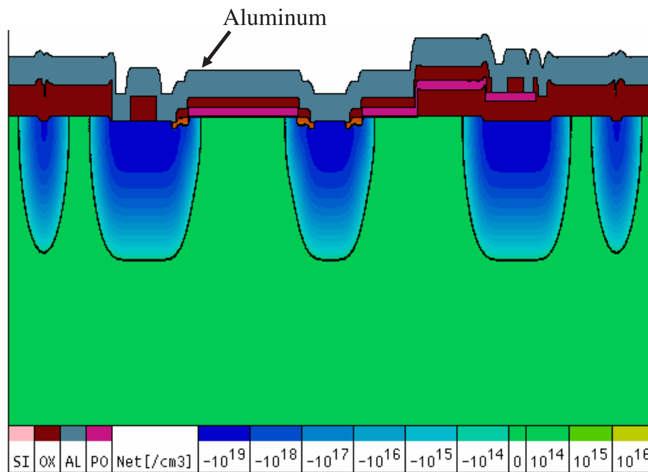


(r) P.R. coating, contact mask for contact open.



(s) P.R. strip and Al deposition.

Fig. 5.34. (*Continued*)

to divert the hole current in the transistor p-base to switch the device operation modes between a thyristor and an IGBT. When Gate 1 is applied a positive voltage and Gate 2 is either applied a positive voltage or is grounded, the device enters the IGBT mode of operation. When the current is sufficiently large to bias the upper cathode junction, the intended thyristor latch-up

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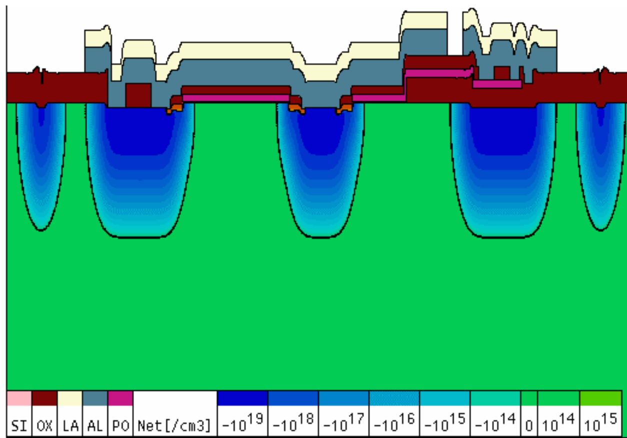
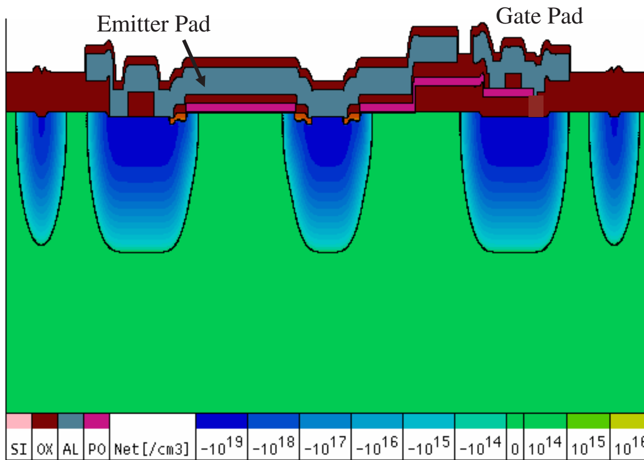


(t) P.R. coating, metal mask, and Al etch.



(u) P.R. strip, alloy sintering, and passivation.

Fig. 5.34. (*Continued*)

occurs. And, the on-state voltage reduces to a lower level, e.g. around 1.1 V at 100 A/cm^2. Published data show that the device can operate at 1.24 V, which is 0.5 V below that of the IGBT device at the current density of 300 A/cm^2 (CSIHPDPIC, 1996). When the device turn-off needs to be made, the operation mode needs to be switched back to the IGBT mode prior to the actual turn-off. When Gate 1 remains at the positive, Gate 2 is applied a negative

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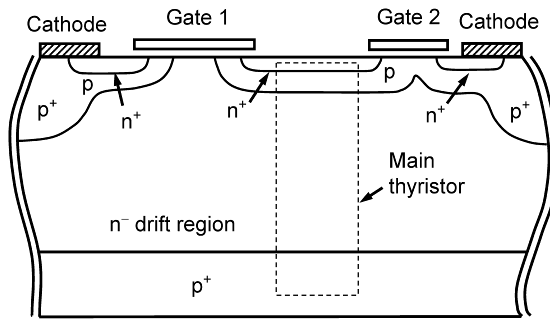

Fig. 5.35. The dual-gate emitter switched thyristor.

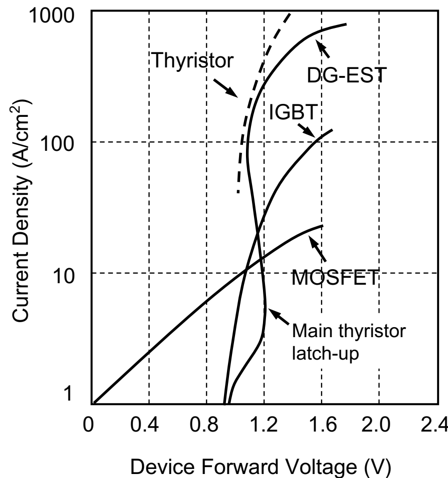

Fig. 5.36. Brief comparison on the on-state *I–V* characteritics of MOSFET, IGBT, EST, and thyristor devices (at 600 V rating).

voltage to turn on the p-MOS channel to divert the transistor base current. This diversion, if strong enough, will lower the upper transistor gain and break the regenerative latch-up. The magnitude of the negative gate voltage applied to Gate 2, ranging from −5 to −20 V, needs to be approximately linearly proportional to the amount of thyristor current to be controlled. When the device operates in the IGBT mode, turn-off can be made by switching off the voltage at Gate 1, as that of IGBT turn-off.

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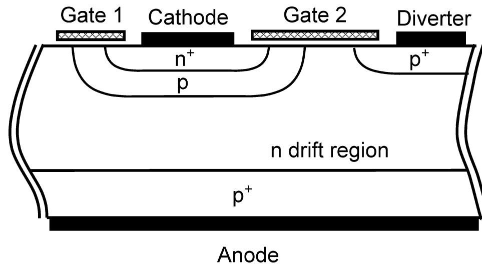

Fig. 5.37. Dual-gate base-resistance-controlled thyristor.

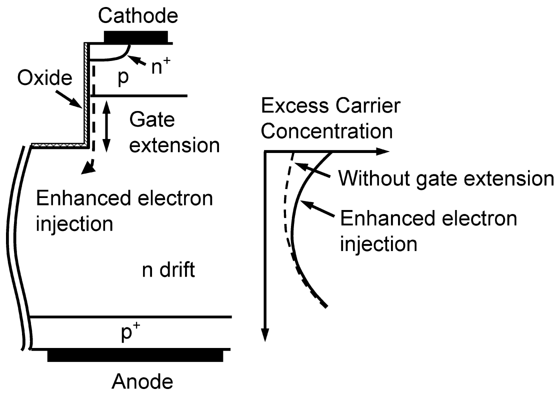

Fig. 5.38. The injection-enhanced IGBT and the excess carrier concentration in the bulk drift region.

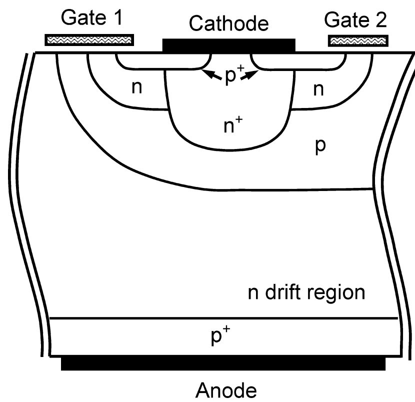

Fig. 5.39. MOS-controlled thyristor.

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5.13.3. Injection-Enhanced Insulated-Gate Bipolar Transistor (IEGT)

The IEGT device was developed to lower the on-state voltage drop (Kitagawa *et al.*, 1993). Of the development, the device rated at 2500 V has a voltage drop of around 4 V at room temperature. The device structure is shown in Fig. 5.38. It has a deep trench with oxide sidewall to inject the electron carriers via the accumulation layer formed by the electric field along the extended vertical gate. The higher amount of electron injection, as shown in Fig. 5.38, raises the electron concentration in the drift region near the p-body then in term it helps to lower the on-state conduction voltage.

5.13.4. MOS-Controlled Thyristor (MCT)

The MCT was developed (Temple, 1984; Bauer *et al.*, 1991) for the similar objectives to have a lower on-state conduction voltage than IGBT devices. The basic device structure is shown in Fig. 5.39 which has both n-channel and p-channel to turn on and to turn off the device. Published data show that a 600 V rated MCT device can be able to carry about 10 times higher current than that of the IGBT device, and about 100 times higher than the MOSFET device (CSIHPDPIC, 1996).

When the Gate 2 is applied a positive voltage, the device functions like an IGBT and due to the prolonged n-emitter, it is very susceptible to latch-up, as an intended characteristic. To turn off the device, a negative gate voltage is needed to be applied to both Gates 1 and 2 to short the upper n^+-emitter/p-base junction, so as to reduce the current gain of n–p–n transistor in order to break the regenerative latch-up. Similar to BRT device, the magnitude of the negative gate voltage should be proportional to the amount of thyristor current to be turned off. CSIHPDPIC (1996) gives the relationship of turn-off current densities and gate voltages for single-cell and array-group of MCT devices. The negative gate voltage varies according to different cell pitches and, for a fixed cell pitch it is almost linearly proportional to the thyristor current density.

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