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CHALLENGES AND PROGRESS IN III-V MOSFETs FOR CMOS CIRCUITS

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An overview of III-V MOSFET technological challenges in comparison to well-established heterostructure-based FET technologies is presented with an emphasis on required properties and possible solutions. Possible approaches to achieve thermodynamically stable high-k gate stack with low interface trap density are reviewed, followed with our results on amorphous Si interface passivation layer (IPL) in-situ deposited on top of GaAs or strained InGaAs MOSFET channels grown by molecular beam epitaxy. Main issues of Si IPL, namely increased equivalent oxide thickness due to IPL oxidation and Si diffusion into the semiconductor channel, are addressed using an *in-situ* deposited HfO_2 with ultrathin (down to 0.25 nm) Si IPL and controlling its bonding state at the interface. Enhancement mode inversion-type MOSFET with HfO_2 high-k oxide is demonstrated. The device employs amorphous Si interface passivation layer, sputter-deposited high-k oxide and metal TaN gate and modulation p-doped GaAs/AlGaAs heterostructure with inversion n-channel formed at the interface with the oxide. The MOSFET with equivalent oxide thickness of 3.7 nm and long 100 μm channel have maximum DC transonductance of 0.9 mS/mm, $I_{on}/I_{off} = 2x10^4$ (at low I_{off} of 30 nA) and effective channel mobility exceeding 1000 cm^2/V-s at sheet electron density $<2x10^{12}$ cm^{-2}.

Keywords: MOSFETs, Gallium alloys, semiconductor-insulator interfaces, mobility.

1. Introduction

Further progress in digital complementary metal-oxide-semiconductor (CMOS) technology is envisioned through improved channel transport and reduction of leakage current through gate dielectrics. These goals strongly inspire the research on group III-V semiconductors for MOS channels integrated with high-k dielectrics.

Though group III-V metal-semiconductor field effect transistor (FET) technology is well-developed, the metal-oxide FETs (MOSFETs) essential for digital circuits are still in an immature phase mainly due to lack of oxide providing thermodynamically stable interface with low density of bandgap states. Fermi level pinning at the interface is a

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major problem in III-V based MOSFETs calling for development of technologies for surface passivation. Uncontrolled oxidation of GaAs surface which results from deposition of almost any oxide on top of it or just exposure to ambient, gives rise to high density of bandgap traps at the interface. To reduce density of the interface states and avoid Fermi level pinning at the III-V/oxide interface, some kind of interface control (or passivation) layer is commonly used. After over 30 years of development of passivation technologies, a significant progress has been achieved, and recently MOSFETs with reasonable performance characteristics have been reported.[1-3]

This paper contains a short overview of III-V MOSFET technological challenges in comparison to well-established heterostructure-based FET technologies. Next, recent progress in interface passivation is reviewed, and followed with our results on amorphous Si interface passivation layer (a-Si IPL) in-situ deposited on top of GaAs or strained InGaAs MOSFET channels grown by molecular beam epitaxy (MBE).

2. MOSFET vs. HEMT

It is worth emphasizing challenges of group III-V MOSFETs by comparison to a mature technology of FETs with Schottky gate, such as metal-semiconductor FET (MESFET) or high-electron mobility transistor (HEMT). MESFET technology is well-developed for digital GaAs circuits,[4] but the most impressive progress has been demonstrated in analog HEMTs. In fact, the HEMT structures with two-dimensional gas separated from scattering ions by modulation doping demonstrated amazing parameters in analog microwave applications, such as channel scalability down to 15 nm, cut-off frequency above 610 GHz of strained InGaAs HEMT,[5] maximum frequency of oscillation of 1 THz of sub-50 nm InP HEMT.[6] The suitability of HEMT technologies for digital CMOS is questionable due to the following issues:

(i) Scaling issues. To maintain the electrostatic integrity of the scaled down FET, the thickness of dielectric or wide-bandgap barrier should be kept low (Fig.1). The ITRS predicts equivalent (k=3.9 as in SiO_2) oxide thickness of ~0.5 nm for gate length of 13 nm for bulk devices or introduction of more efficient wrap-around gate geometries, such as Intel's tri-gate transistors. Fabrication of a Schottky metal gate within ~1.5nm (given k~9-12 for semiconductor) from the 2D gas is a big challenge for HEMT technology due to increased leakage current through a Schottky junction.

(ii) Power issues. The gate leakage is significantly higher in Schottky junction than in a MOS stack and is further increasing rapidly with scaling. The gate leakage also increases the I_{off} current of the transistor.

(iii) Need of enhancement mode / inversion channel. CMOS circuits are based on enhancement mode (e-mode) (normally off) transistors built typically with inversion channel in Si or SiGe. Though fundamentally not necessary for CMOS, inversion-type channel allows for a greater versatility of building CMOS circuits, for example, making both n-channel and p-channel transistors in the same heterostructure and automatically providing e-mode operation. HEMT can be considered an accumulation type device as it uses majority carriers produced by doping in the barrier, and the Fermi level in n-channel

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device is located in the upper half of the bandgap in the absence of the field, and most importantly the conducting channel is formed without high transverse electric field typical for inversion. The e-mode HEMTs are also well-developed. In these devices, channel depletion at zero gate voltage is a result of high built-in Schottky barrier. Pt-based gate metal[7] and wide-bandgap barrier material, such as InAlAs instead of InGaAs on InP substrate and AlGaAs instead of GaAs on GaAs substrate,[8] are typically used to increase the gate Schottky barrier above 0.9-1.1 V. Contrary to the HEMT with built-in majority carrier channel and wide access regions, the inversion channel MOSFET is significantly more compact but requires contact implantation overlapped with the gate as shown in Fig.1.

(iv) Issues with a recessed gate. Non-self-aligned recessed gate technology is a great approach which is responsible for HEMT progress due to relative ease of short gate fabrication and low source/drain resistances formed on a highly-doped semiconductor layer as shown in the Fig.1. On the other hand, this technology is hardly useful for digital VLSI owing to large variations of the threshold voltage across the wafer as a result of recessed gate process deviations, large footprint of HEMT unacceptable for real estate-hungry VLSI and also resulting in higher parasitic capacitance.

Currently, there are significant efforts to adopt HEMT technologies in CMOS applications with impressive improvements[9] to overcome intrinsic problems of HEMTs, such as scaling and low On/Off current ratio. It is also clear that MOSFET would be a superior device for CMOS if existing problems are solved.

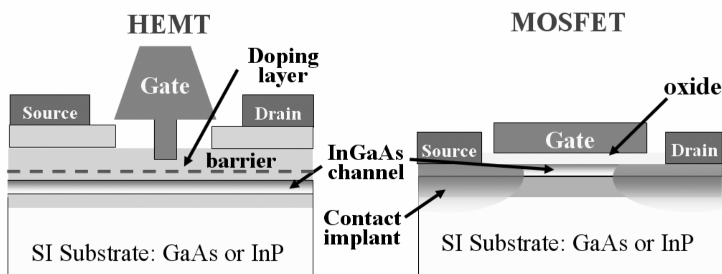

Fig.1. Typical T-gate HEMT (left) and MOSFET (right) layouts.

3. Wish List for III-V CMOS

Based on the comparison with mature HEMTs, it is now easy to compile a list of essential requirements for III-V MOSFETs technology to be employed in CMOS circuits (Table 1). Naturally for any technology, improvement of one parameter (say channel mobility in a buried channel) results in degradation of other parameters (e.g. increase equivalent oxide thickness), therefore choice of design and technology is a subject of trade-offs and optimization.

Superior electron transport properties are a major reason why III-V's are considered for advanced CMOS circuits. However, placing the semiconductor channel in close

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proximity to a high-k gate oxide reduces mobility significantly in a similar ways as in Si channel due to interface roughness and soft phonon scattering. Reduction of these scattering mechanisms may be achieved by inserting of a 3-10 nm thick wide-bandgap semiconductor barrier spacer between the channel and oxide. But this approach adds to the equivalent oxide thickness and reinstates the scaling issues as in HEMTs. Quite obviously optimization of the spacer layer can be obtained for a particular FET design and generation.

Another important requirement for III-V CMOS technology is a high-mobility p-type channel matching within a factor 3-5 the mobility of an n-channel. The major competitor for p-channel is strained germanium with bulk room temperature hole mobility of 1900 cm^2/Vs. Due to polar nature of III-V's, their hole mobilites are much less (400 cm^2/Vs in bulk GaAs) and are determined by polar optical phonon scattering at room temperature. The III-V mobility can be improved in compressively strained quantum wells via splitting of heavy and light hole subbands. But there is no way the III-V hole mobility can exceed that of strained Ge. On the other hand, the high mobility (low scattering) requirement is essential to the drift channels, and will be likely eased up in ballistic channels below ~10nm.

Table 1. Wish list for III-V CMOS Technology.

Properties	Issues	Approaches
Thermodynamic stability of gate stack	~800^0C for implant activation.	Oxides preventing interdiffusion. Ref. 2,3,10
Low interface trap density (D_{it})	Typically high D_{it} for III-V's results in Fermi-level pinning, large subthreshold swing voltage.	Interface passivation. D_{it} below 10^{11} $cm^{-2}eV^{-1}$. [11]
High drain current	HEMT-like structure with buried channel and wide-bandgap barrier between the channel and the gate increases EOT.	Buried channel, mobility above 5000 cm^2/Vs and channel sheet resistance 430 Ω/sq.[1]
Low source/drain resistance	Low-area ohmic contacts and access region resistance should be improved for further scaling.	Implanted source-drain[2] or highly-modulation-doped channel[1.] give ~0.5 Ω-mm, semiconductor regrowth further improves S-D resistance down to 0.01-0.02 Ω-mm.
Inversion channel	Need of implanted source/drain, higher scattering of minority carriers due to higher effective field.	Ref .2, 3, 24, 39, 40
Low EOT and low gate leakage	Scalability, electrostatic integrity. Buried channel increases EOT.	High-k gate dielectrics, 1.6 nm for 10 nm HfO_2.[12]
p-channel	Low hole mobility due to polar optical phonon scattering and large hole mass.	Strained channel to split heavy/light holes.

4. Interface Passivation Technologies

Surfaces of group III-V semiconductors typically contains high density of traps resulting in Fermi level pinning and high surface recombination rates. It is typically accepted that

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these midgap traps are associated with surface oxidation (possibly with As-O bonds[13]), and are present at almost any interface with a metal or dielectric. This problem can be addressed by appropriate interface control using some sort of surface passivation. After more than three decades of research, a large number of passivation techniques were proposed and tested (Table 2).

In 90's and early 00's, mainly due to the efforts of researchers from Bell Labs and later Motorola, $(GaGd)_2O_3$ gate oxide was positioned as the most promising material for III-V interface passivation, possibly due to formation of electrically inert bonds at the interface, such as Ga-O-Ga rather than As-O.[13] Atomic layer deposition (ALD) which is currently a mainstream technology for high-k gate stacks on Si is also very attractive for III-V's, as it may not need any special passivation[19,38] (although sulfur[22] or Si[23] passivation might be still beneficial). We have recently reported on effectiveness of a 1.5 nm thick amorphous Si interface passivation layer (IPL) for *in situ* passivation of GaAs and InGaAs surface enabling good electrical properties and thermal stability with high-k oxide.[17] Further improvements and mainly in-situ deposition of high-k oxide, resulted in virtually zero thickness of Si IPL.[12,16]

Table 2. Interface Passivation Technologies

Passivation Technology	References
In-situ high-k oxide on InGaAs	Ref. 16
Amorphous ultrathin Si or Ge	Ref. 3,17-19
Atomic layer deposition of Al_2O_3, HfO_2	Ref. 20-23
E-beam or MBE of Ga_2O_3–Gd_2O_3	Ref. 11,24-27
MBE -grown crystalline silicon	Ref. 28-30
Atomic layer passivation with InP or GaP layers	Ref. 31,32
Sb-passivation of GaAs with MgO dielectric	Ref. 33
Low-temperature-grown GaAs	Ref. 34
Sulfur, Na_2S , $(NH_4)_2S$ passivation	Ref. 22,35
Hydrogen or Nitrogen plasma treatment	Ref. 36,37

5. Amorphous Si Interface Passivation Layer

Recently, we have shown that an *in-situ* deposited amorphous Si interface passivation layer (IPL) of at least 1.5 nm thickness can be used to reduce interface state density and prevent the Fermi level pinning at GaAs or InGaAs interface with an *ex-situ* high-k HfO_2 deposited by magnetron sputtering.[17] An unpinned Fermi level was demonstrated (Fig. 2a) when Si IPL prevented oxidation of arsenic during exposure to atmosphere and oxide deposition. Structure and chemistry of the interface between GaAs and Si IPL has been recently studied using XPS and TEM.[3] A 1.5 nm thick IPL used in the gate stack was found to consist of amorphous Si-As alloy with 30-50 atomic % of As. It was oxidized throughout almost its entire thickness but contained a fraction of covalent Si at the

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interface with GaAs. The presence of unoxidized Si at the interface and the absence of As-O bonds in GaAs was correlated with unpinned Fermi level in MOS capacitors.[17]

A significant drawback of the sputtered oxide is a large hysteresis close to 1 V observed on MOS capacitors fabricated on top of n-GaAs layers (Fig. 2a). It can be further argued that the charge captured in the oxide is responsible for the hysteresis, as the hysteresis is proportional to the oxide thickness and is reduced down to 0.25 V in the structure with a 4 nm - thick HfO_2.

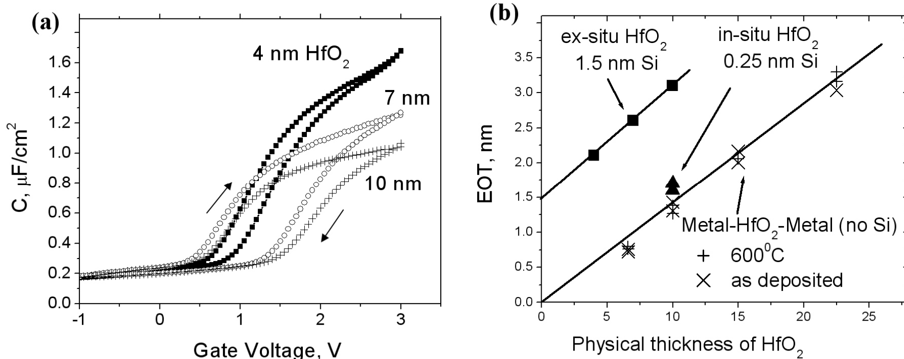

Fig. 2. (a) 1 MHz capacitance-voltage characteristics of GaAs/HfO_2 MOS structures with 1.5 nm thick *a*-Si IPL. Hysteresis is proportional to oxide thickness, indicating charge trapping in HfO_2. (b) Dependence of the equivalent oxide thickness (EOT) on physical thickness of HfO_2 for MOS structures with 1.5 nm and 0.25 nm thick Si IPL. Crosses correspond to Ni-HfO_2-TaN capacitors. EOT is reduced down to 1.6 nm compared to ex-situ deposited oxide. EOT scaling corresponds to HfO_2 dielectric constant k = 23 and ~1.4 nm offset mostly due to oxidized IPL.

Another important feature of this gate stack is reproducibility of electrical results which is indicated by a linear scaling of EOT with HfO_2 thickness (Fig. 2b). The slope of this line corresponds to the dielectric constant of 23, and ~1.4 nm offset is consistent with the thickness of the oxidized IPL within the accuracy of measurements. The n-GaAs MOS capacitors with 1.5 nm Si IPL demonstrated a maximum accumulation capacitance of 1.6 $\mu F/cm^2$ corresponding to EOT of ~ 2.2 nm.

To reduce the EOT we were further able to use ultrathin *a*-Si IPL scaled down to 0.25 nm with *in-situ* grown HfO_2 (Fig.3). In this case, after the completion of the MBE growth of the III-V group materials and amorphous Si IPL, a HfO_2 gate oxide was deposited in the same ultrahigh vacuum system using reactive electron beam evaporation at room temperature at oxygen pressure of 3 x 10^{-6} Torr. The details of the *in-situ* growth conditions for Si IPL and HfO_2 are described elsewhere.[3] *In-situ* deposition of the oxide prevented the exposure of the semiconductor structure with IPL to atmosphere and thus reduced the native silicon oxide thickness due to the environmental oxidation.

By comparing the EOT for samples with *ex-situ* and *in-situ* grown HfO_2, (Fig. 2b) we found that the contribution of the interfacial passivation layer to EOT could be reduced by ~ 1.3 nm, approaching the value obtained on the metal-oxide-metal (MOM) structures without any interfacial layer. The dielectric constant of the e-beam deposited *in-situ* HfO_2

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was found to be ~26 as measured on Ni-HfO_2-TaN MOM samples with scaled oxide thickness (Fig. 2b).

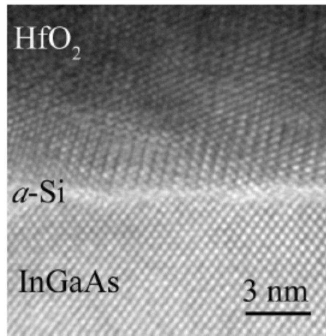

Fig. 3. High-resolution TEM image of in-situ deposited *a*-Si IPL scaled down to 0.25 nm.

As discussed above, thermal stability of the gate stack is essential due to a relatively high processing temperature of MOSFETs to activate ion-implanted impurities. We have found that the stacks with thick Si IPL are in general less thermally stable against Si diffusion into semiconductor than those with thin IPL. The diffusion of Si into n-GaAs results in the increase of the donor concentration in the semiconductor. It is clearly observed via the rise of high-frequency capacitance in deep depletion when a sample is annealed above 650 ^{0}C. Another even more notable effect is an inversion of the conductivity type from p-type to n-type after annealing as shown in Fig. 4(a). Remarkably, Si diffusion can be suppressed if the IPL thickness is reduced (Fig.4b) and its bonding status with oxygen and arsenic at the interface is controlled.[17] We believe that in the latter sample with 0.5 nm – thick IPL silicon is almost entirely oxidized, and therefore, bound to oxygen resulting in suppressed diffusion. In contrast, samples with excess IPL thickness containing unoxidized Si exhibit Si diffusion at implant activation temperature.

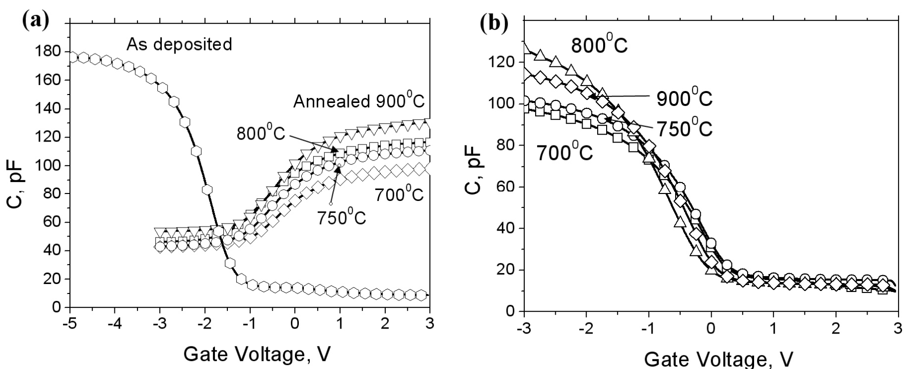

Fig. 4. 1 MHz capacitance-voltage characteristics of p-doped GaAs MOS capacitors with (a) 1 nm and (b) 0.5 nm amorphous Si IPL. Inversion of conductivity due to Si diffusion into semiconductor is observed at annealing temperature >650 ^{0}C on samples with thicker Si IPL. Change of accumulation capacitance is likely due to a densification of oxide.

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6. Enhancement- Mode Inversion-Type MOSFET

Both depletion mode and enhancement mode (d-mode and e-mode) transistors were fabricated using Si IPL.[3,12,23] For e-mode devices, self-aligned Si^+ ion implantation into the source and drain regions to a dose of 10^{14} cm^{-2} was used. Implanted species were activated by rapid thermal annealing at 700 ^{0}C for 30 sec. Although this post implantation anneal was expected to activate only a few percent of implanted impurities and result in high series resistance, low annealing temperature was chosen to prevent possible degradation of the gate stack. Au-Ge based Ohmic contacts were deposited onto the source and drain regions using a separate mask with 10 μm gaps between a contact and the gate. To minimize the effect of source-drain resistance we also measured large ring-shaped FETs with a gate length over 100 μm.

The interface quality is best characterized by the parameters of inversion-type MOSFETs with interface channel generated solely by field effect. In this case, the 2D carrier gas is strongly localized at the semiconductor/oxide interface by the electric field resulting in a significantly increased effect of interface scattering as compared to accumulation - type channel devices no matter whether or not they are depletion or enhancement mode. Though first inversion MOSFETs were demonstrated over three decades ago,[14,39] only recently transistors begin to show reasonable characteristics.[2,23,24] In the present paper, we demonstrate enhancement mode inversion – type GaAs n-MOSFET with inversion interface channel with HfO_2 gate oxide and TaN metal gate.

For e-mode MOSFET we used an MBE grown modulation doped structure consisting of a 70 nm thick undoped GaAs channel on top of a 100 nm thick $Al_{0.3}Ga_{0.7}As$ barrier grown on semi-insulating GaAs wafer with a buffer layer (Fig. 5a). An undoped $Al_{0.3}Ga_{0.7}As$ 5 nm-thick spacer separates the channel from 30-nm thick portion of the barrier doped with carbon to p=2×10^{17} cm^{-3} to compensate for possible background doping of the GaAs channel. Such modulation doping should result in a sheet holes concentration of 7×10^{11} cm^{-2} in the channel at flat-band condition. Modulation doping was chosen in order to increase electron mobility in the channel by eliminating electron scattering by ionized impurities.

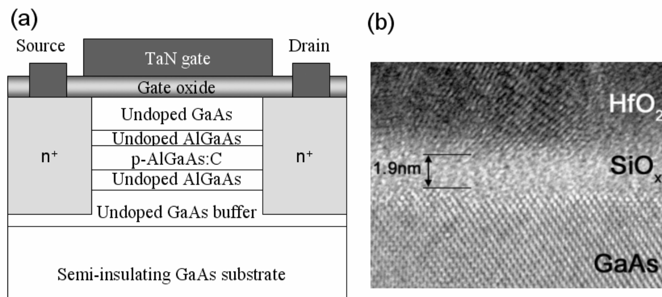

Fig.5 (a) Layout of an enhancement-mode GaAs n-MOSFET with *a*-Si IPL and HfO_2 as a gate oxide; (b) High resolution cross-sectional TEM of GaAs/SiO_x/HfO_2 interface.

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A high-resolution TEM image of the gate stack (Fig. 5b) shows the interface between GaAs channel and high-k oxide with intermediate oxidized a-Si IPL. In this case, the gate consisted of a 1.5 nm - thick *in-situ a*-Si IPL with about 12 nm-thick *ex-situ* grown HfO_2.

Figs. 6 and 7 show electrical characteristics of the MOSFET. Gate leakage current density (Fig.6a) was reasonably low for 12 nm-thick HfO_2, which gave the equivalent oxide thickness (EOT) of 3.7 nm as determined from the measurements of gate capacitance from split C-V characteristics. The leakage current was found to increase significantly in the gate stacks annealed above 750 ^{0}C for *ex-situ* grown HfO_2. This observation prevented us from use of higher temperature post-implantation anneal required for effective activation of dopants in the source and drain regions. Output I-V characteristics of a long channel MOSFET are shown in Fig. 6(b) and correspond to operation of MOSFET with n-channel with the threshold voltage close to zero. The slope of the linear part of these characteristics saturates at V_g above 1.5 V indicating high source and drain resistances of about 2 kΩ likely due to the mentioned low-temperature post-implant annealing.

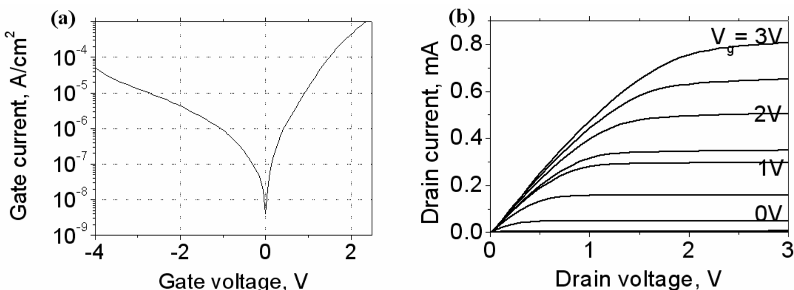

Fig. 6. Electrical characteristics of inversion-type GaAs n-MOSFET: (a) Gate leakage current density vs. gate voltage; (b) Drain current vs. drain bias as a function of gate voltage.

Drain current versus gate voltage characteristics are shown in Fig. 7(a) on semi-logarithmic scale to highlight the subthreshold characteristics of the device. A disappointing feature is a large hysteresis (threshold voltage V_t = -0.1 +0.6), which in this case represented via variation of the gate voltage span. As shown above, the hysteresis was found to be significantly less in the structures with thinner HfO_2, down to 0.25 V for 4nm - thick oxide (Fig. 2).

The highest transconductance of 0.9 mS/mm was measured for 100 µm channel at the drain voltage of 4.5 V. For comparison purpose, it is worth giving an intrinsic transonductance scaled to 1 µm channel, 90 mS/mm. This value is 3 times lower than that obtained on a depletion mode n-MOSFET with Si IPL and 3.6 nm thick HfO_2 gate oxide (270 mS/mm scaled to 1 µm gate length).[3] These results just illustrate a significantly stronger influence of the interface scattering on the inversion channel than on the built-in or accumulation channel. In any case, to the best of our knowledge the demonstrated intrinsic transconductance is the highest ever reported for the GaAs interface inversion channel. Of course, the channel conductance can be improved in a buried channel at the expense of increased EOT, which might be detrimental for short channel electrostatic integrity.

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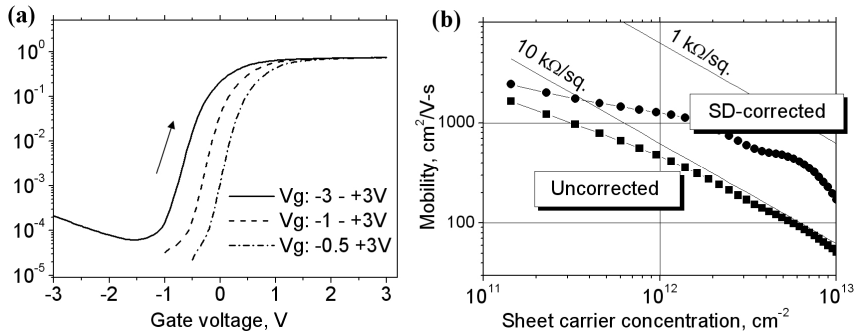

Fig. 7 (a) Drain current vs. gate voltage for different voltage span at the drain bias of 1V. Subthreshold swing is 170 mV/dec, increase of the drain current at negative gate voltage is due to the gate leakage. (b) Effective electron mobility as a function of electron sheet density. As-measured and corrected for source-drain resistances curves are presented. Sheet resistance curves are plotted as a guide.

To illustrate the conductance behavior, effective channel mobility as a function of electron sheet density is plotted in Fig.7b. Effective electron mobility of the channel is calculated, using sheet electron concentration measured from C-V characteristics and drain current. The maximum inversion sheet carrier concentration was as high as $N_s=10^{13}$ cm^{-2} as calculated by integrating a C-V curve of the MOSFET with shorted source and drain. This concentration is likely to be overestimated due to relatively high interface trap density. Source and drain resistance was estimated to be very high, 1.7 kΩ-mm, due to insufficient implant activation. This called for the measurements using long-gate transistors to reduce the effect of source and drain resistances. The Fig. 7b shows also the effective channel mobility curve corrected for the source and drain resistances. Sheet resistance curves proportional to $1/(\mu N_s)$ are plotted as a helpful guide. The maximum effective channel electron mobility μ was close to 2000 $cm^2/V \cdot s$ at low sheet electron densities, but dropped rapidly at higher carrier densities. However, we believe that the presented curves for mobility underestimate this value at higher densities due to overestimation of the mobile carrier density from C-V curves in the presence of the interface states. The intrinsic channel parameters are significantly higher than reported previously for GaAs inversion surface channels,[24,39,40] and are similar or better than that of InGaAs surface channel with the most recent ALD grown Al_2O_3 gate oxide.[2]

7. Conclusions

A mature III-V Schottky gate FET technology, such as HEMT, is likely unsuitable for CMOS as shown by the analysis of CMOS technology requirements. The major challenge towards the improvement of MOSFETs with III-V channels is a technology for thermodynamically stable high-k gate stack with low interface trap density. One of the possible solutions is an interface passivation scheme using *in-situ* deposited amorphous Si interface passivation layer. The main problems of Si IPL, namely increased equivalent oxide thickness due to IPL oxidation and Si diffusion into the semiconductor channel, were solved using an in-situ deposited HfO_2 with ultrathin (0.25 nm) Si IPL. An *in-situ*

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HfO_2 deposition was applied to scale down of the Si IPL thickness resulting in reduction of equivalent oxide thickness down to 1.6 nm for 10 nm thick HfO_2 layer. Reduction of the Si IPL thickness along with the control of its bonding status also results in higher thermal stability of the gate stack against Si in-diffusion.

Enhancement mode inversion-type MOSFET with HfO_2 high-k oxide is demonstrated for the first time. The MOSFET with equivalent oxide thickness of 3.7 nm and long 100 μm channel devices had maximum DC transonductance of 0.9 mS/mm (corresponding to intrinsic transonductance of 90 mS/mm scaled to 1 μm channel), I_{on}/I_{off} = 0.7 mA/30 nA, and threshold voltage of as high as +0.6 V (affected by the oxide hysteresis). Effective channel mobility exceeding 1000 $cm^2/V\text{-}s$ at low sheet electron density ($<2x10^{12}$ cm^{-2}) was demonstrated. This results in the sheet channel resistance of 3-10 kΩ/sq. for an open transistor.

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