CHAPTER 1
Introduction

1.1 What is Electromigration?

Electromigration is the phenomena of interconnect metal self-diffusion along an interconnection as high current density is passing through the interconnection. As a result of the metal movement, voids will be formed on some parts of the interconnection, and hillock due to the accumulation of the metal atoms will be formed on different parts of the interconnection. The presence of voids will increase the resistance of the interconnection, and the presence of hillock will cause short circuit between the adjacent interconnections if the hillock is developed side-way and short circuit between the different levels of interconnections if the hillock is developed vertically and punch through the inter-metal dielectric.

Electromigration has been a subject of scientific study for over 100 years, but the interest remained academic until it became a major failure mechanism for integrated circuits (IC) in 1959 as thin and narrow metal films are used for interconnections. Indeed, electromigration was the one of the first few failure mechanisms found in IC.

Unlike the bulk conductor which will melt from Joule heating at $\sim 10^4$ A/cm^2, the metallization in IC can sustain current densities greater than 10^7 A/cm^2 due to the good thermal contact with the silicon substrate. It is this high current density that makes the effect of electromigration becomes significant.

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In addition, thin film interconnections in IC possess small grain sizes and high surface or interfacial area to volume ratios with many high mobility diffusion paths, allowing mass transport of the self-diffused metal atoms at low temperatures. When these diffusion paths intersect with one another, and each having different mobility, accumulation of atoms or voids nucleation will results at the intersection. This combination of a high driving force for electromigration and the availability of inhomogeneous high-mobility diffusion-paths network makes thin film conductor susceptible to electromigration damage.

1.2 Importance of Electromigration

With the technology scaling according to the International Technology Roadmap for Semiconductors (ITRS) 2007, the geometrical dimensions of transistors and interconnects decrease linearly. On the other hand, supply voltage scaling is saturating. These different scaling trends increase the electric fields. Furthermore, new materials, such as the porous low-k materials and Cu are introduced to meet evolving technologies requirements. As a result, effects that were considered to be second order in previous technology nodes, such as reliability, are becoming important considerations during IC design (Papanikolaou 2006). For example, electromigration continues to worsen due to smaller interconnect width and thickness as well as smaller separation between interconnections. As a result, coalesce of fewer vacancies can cause unwanted significant via resistance rise. Time-dependent dielectric breakdown happens much more often because of lower k materials with the worse breakdown behavior (McPherson 2007).

Interconnect reliability, with electromigration as the dominate failure mechanism, is the main factor that determines the circuit reliability especially when the line width becomes much narrower that renders high current density as shown by Srinivasan (Srinivasan 2004). They showed that the failure rate of a scaled 65 nm processor is more than three times higher than a similarly pipelined 180 nm processor, with electromigration (EM) and time-dependent dielectric breakdown showing the most dominant mechanisms with the advancement in the technology nodes. The increasing failure rate is believed to be due to the potentially shorter time to failure of an interconnection with narrower line width and the increasing sensitivity of the circuits to interconnect line resistances as the circuits are operating at

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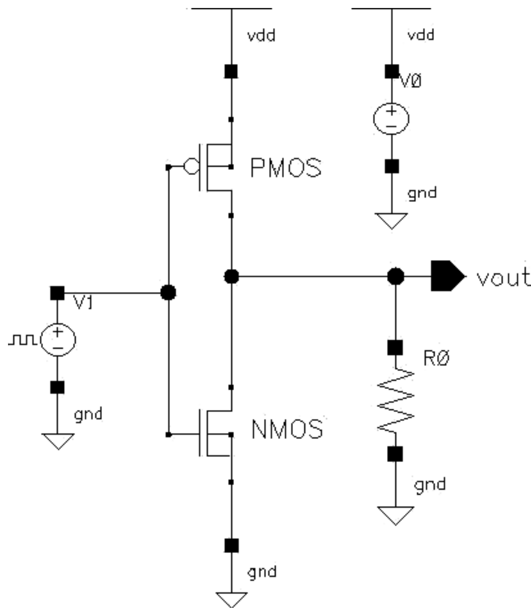

Fig. 1.1. Schematic of a simple inverter circuit to illustrate the increasing sensitivity of circuit performance to interconnects resistances.

higher frequency. For illustration purpose, we study a simple CMOS voltage inverter circuit as shown in Fig. 1.1.

We model interconnects in the circuit as resistors whose values will increase with time due to electromigration. Figures 1.2 and 1.3 show that the higher the interconnect resistance, the worse the circuit performance, i.e. longer signal delay and higher power consumption, and such impact of interconnect resistance to IC performance is greater as the operating frequency of the integrated circuits became higher.

Also, with the same simulation setup using Cadence EDA tool, when the circuit operating frequency increases (e.g. from 100 MHz to 1 GHz), the resulting temperature of the circuit increases as can be seen from the temperature extrapolation in Fig. 1.4 using ANSYS finite element modeling.

The increase in the circuit temperature as shown in Fig. 1.4 will increase the electromigration degradation rate (Cher Ming Tan; Roy October 2007), thus shorten the life time and degrade the reliability of an integrated circuit.

From the above discussion, it is obvious that the study of interconnect reliability in an integrated circuit is increasingly important as technology

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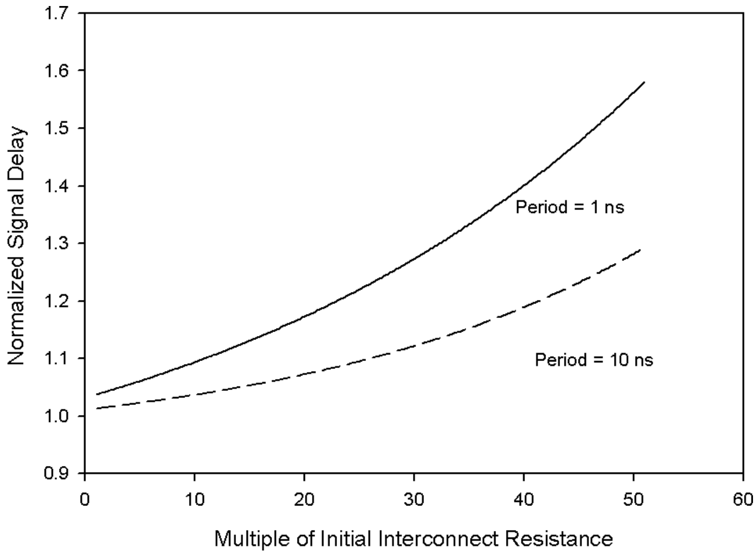

Fig. 1.2. Effect of interconnect resistance on signal delay under different operating frequency. (Initial % signal delay for 10 ns period = 0.8%; for 1 ns period = 4%).

node advances in order to ensure its reliability. This concurs with the recent work by Guo *et al.* (Jin Guo December 2008).

In fact, chip failures due to power grid issues, whether IR drop or electromigration, are already being discovered by chip designers. Since these issues are related to the number and the way components are assembled on a chip and are primarily a global phenomenon, power grid analysis is becoming a required addition to many design flows (Cooke, Goossens *et al.*). This, together with the rapid evolution of technology scaling, does not allow needed time for proper thorough evaluation of new interconnection reliability, thus additional efforts at the design stage are essential now to obtain robust and reliable chips (Guo, Papanikolaou *et al.* 2008).

In order to provide adequate knowledge on the interconnect electromigration for both the IC manufacturers and designers, a comprehensive monograph on electromigration for ULSI Interconnections covering the physics of electromigration, the various factors, both process and design related, that can influence electromigration, the testing methodologies of interconnect reliability and the modeling of electromigration is necessary. It is to these purposes that this monograph is written.

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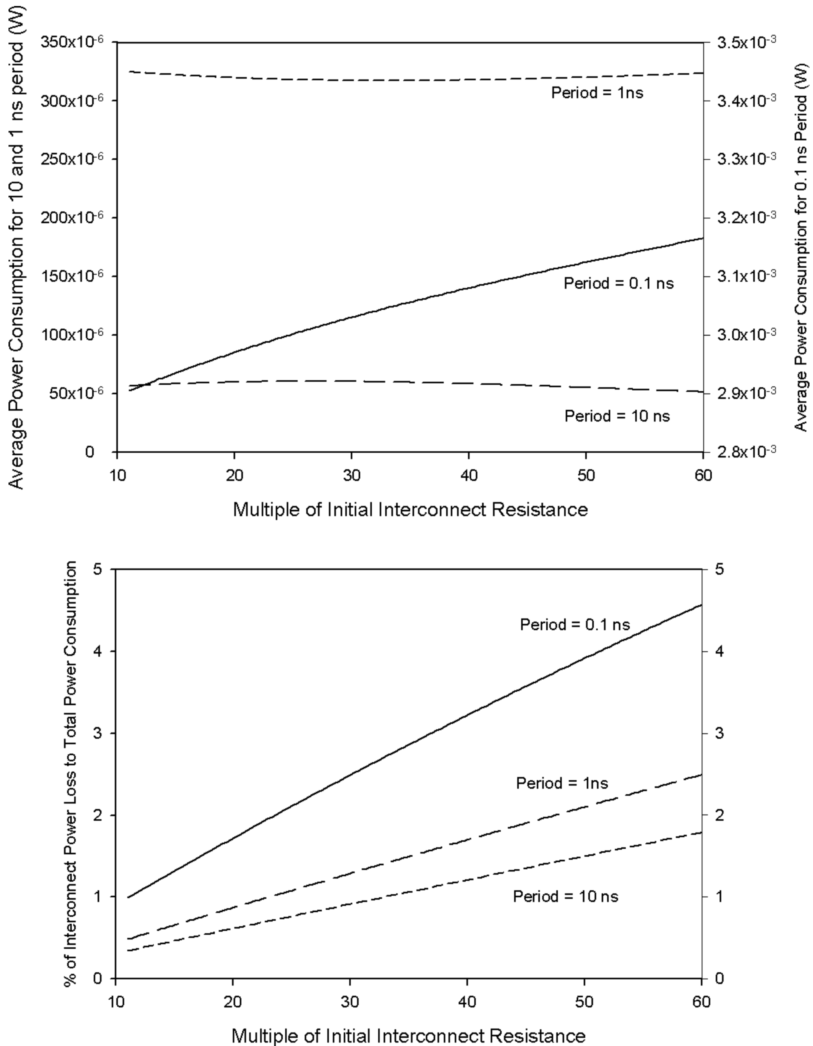

Fig. 1.3. Effect of interconnect resistance on circuit power consumption under different operating frequency. Note that the right vertical axis of the left figure is for the case of circuit operating at 1 GHz.

The modeling of electromigration is particularly important because it helps to identify the critical weak spots of an interconnection system in a short time. A typical IC layout has millions of interconnects. Analyzing the reliability problems on each of them is prohibitively time consuming.

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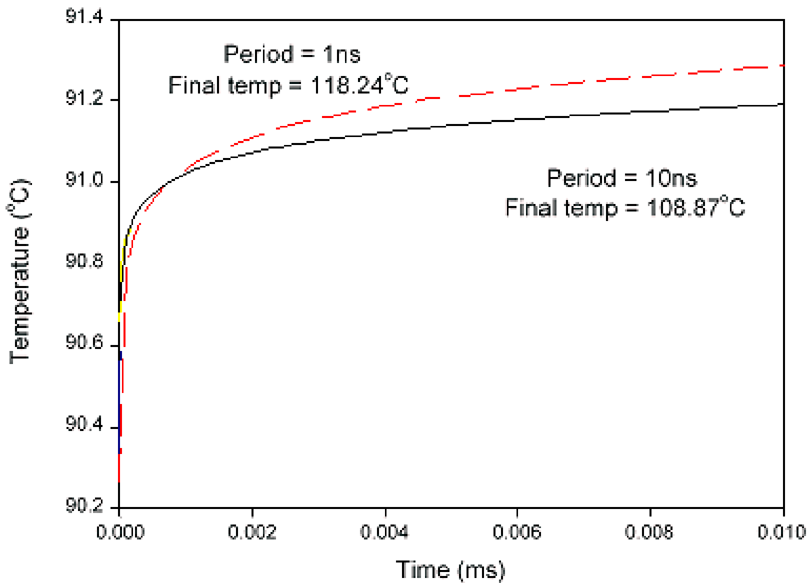

Fig. 1.4. Time variation of the temperatures of the circuit operating at different frequencies.

Therefore, the key interconnects which will be investigated will have to be identified through electromigration modeling. Also, if the modeling of electromigration can be integrated into EDA tool, a complete electromigration aware IC design can be realized.

1.3 Outlines of this Book

Since the discovery of electromigration (EM) phenomena in the 60's, the theory of EM revolved around the electron wind force as it was identified to be the sole driving force responsible for the EM failure observed in interconnects. This electron wind force formulation by Fiks (Fiks 1959) and Huntington and Grone (Huntington and Grone 1961) is a major contribution to the study of EM, and it has explained many experimental EM observations in Al interconnect. Later on, Black developed an empirical equation to relate the median time to failure with respect to the current density and temperature of the metal interconnects (Black 1967), and has been widely used till now.

With the various interconnect system developed, and a continuous shrinkage of the interconnect line width as well as the change in the interconnect material, the theory of EM is being refined and driving forces

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other than the electron wind force are found to be significant, and the correctness of the Black equation in predicting the median times to failure of interconnect is also become questionable. In this work, the evolution of the physical theory of EM will be explored, and both the diffusion path and driving force approaches in EM study will be discussed. The continuous interaction of the various driving forces during the EM process will be shown.

While the basic of EM is the metal atoms movement under driving forces through various diffusion paths in the metal interconnection, the changing dominance of the driving forces and the diffusion paths due to the design and process of an interconnect system complicate the understanding of the EM physics. Fortunately, with the advancement in numerical tools, our understanding of the underlying physics is enhanced, and key factors that affect the EM performances of an interconnect system can be identified. This is significant for ULSI development so that a reliable interconnect system can be built as ULSI technology is advancing.

Various numerical schemes such as finite-element-analysis, solution of coupled diffusion equations for EM etc. have been developed and will be presented in this work. The advantages, disadvantages, achievement and correlation of these models to the experimental results will be discussed. Some quantum mechanical treatments of the phenomenon and their short-comings will also be presented.

EM testing is essential for all wafer fabrication plants with interconnect back end of line (BEOL). Various test structures have been developed and used in the last two decades for EM testing, and they will be presented. As the interconnect technology is improving, the required time of EM testing is getting longer, and different type of accelerated tests are developed in both academic and industrial. Some of these accelerated tests however, do not produce results that can help in predicting the life time of an interconnect system under normal operation condition, and in some cases, they can even produce misleading information. Their problems stem from the improper test structure design, incorrect use of stress conditions and inaccurate test data analysis methods used. All these problems will be discussed in detail so that a rigorous accelerated stress testing for EM can be established.

Physical failure analysis is the postmortem of EM experiments. Methodology that can reduce the required resources for physical analysis

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will be presented. Non destructive techniques to detect the failure locations and their capability will be presented.

With the vast amount of knowledge on Al EM, extension of this knowledge to the present Cu interconnect will be presented, and the differences in the EM behaviors for Al and Cu will be highlighted and explained in relation to their different process technologies. The various processes and materials related improvement for interconnect EM will be reviewed. The current progress and outstanding issues on Cu EM characteristics will be addressed, and the different key factors that influence Cu EM will be discussed in details. The sources of these factors and their interaction will be explored, and their effect on the EM activation energy, void locations, void growth and void nucleation dominated mechanisms will be discussed. The understanding of these sources from design and process perspective will be helpful in the design of Cu interconnect system. Environmental related factors are also considered so that the EM performance of Cu based interconnect system can be accurately assessed.

As the ULSI technology is advancing, and the demand for ULSI in term of speed and functionality are ever increasing, the interconnect system is facing a number of different challenges ahead. Novel interconnect systems such as 3D interconnect are proposed and experimented, new interconnect materials are also being explored. The reliability of these new proposals remains unknown, and in the last section, the potential reliability problems for these new proposals will be outlined and discussed.

The structure of the book is organized as follows. We begin the description of the history of EM in Chapter 2. We then proceed to describe the various experimental studies of EM for Al and Cu respectively in Chapters 3 and 4 where the test structures used for EM, the test methodologies, the failure analysis methods for EM failures, the reported experimental results for EM as well as the data analysis of the time to failure for EM test will be discussed. With these experimental findings, a much better understanding of the physics of EM is obtained and hence a physics based numerical modeling of EM is possible, and it enables us to identify the design, process and material related factors that govern the EM of interconnects which will be useful for both the foundries and IC designers. The various numerical modeling for EM will be described in Chapter 5. Lastly, the future challenges in interconnect EM will be discussed in Chapter 6.

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