Foreword and History

I will not practice here what I preach, on limiting the Foreword to one book page, as I have managed to do for the previous four monographs of this series on device modeling. I would like to use this rare opportunity, because, I think there is an interesting story and a relevant history to tell, on how things are developed. It proves the thesis: Progress is made via generations of **natural Darwin evolution** and **artificial evolutions**-or-**intelligent designs**. Intelligent designs feed evolution, which in turn furthers design intelligence, providing the positive feedback loop that perpetually speeds up the cycle. It can be a cycle as long as many hundreds thousands of years or many human lifetimes, to the longer biological evolution times. It can become as short as one, two or three years, only about a tenth of the thirty-year human generation, such as the Gordon Moore Law. The increasing acceleration is the result of human intelligence learned and built up from many generations of evolution, the route with the positive feedback loop.

Although in the traditional or recent statistical sense, my samples are very small, they are real data, not random statistical spikes. Their impacts and consequences have affected the ~six billions as well as also all the rest of the trillion trillions evolved and evolving beings. Therefore, they cannot be just statistical random fluctuations or random spikes above the noise in the background. These examples have each one or more significant if not dominating components of artificial intelligent designs, accomplished by evolving educated and learned minds in three to five human generations, from grandparents to grandchildren, and from teachers to students.

The stories are stories of Electromigration, the subject of this book. They are described in this extended Foreword, re-titled Foreword and History. After you read this Foreword and History, I hope you will agree that the case histories you have just read show that evolution and intelligent design are in fact two of the same in a broader perspective. To wit, as we evolve, we recognize we have actually designed the evolution by our intelligence, which has sped up the evolution. The evolution then drives the intelligence to become more learned, nurtured, and grown under controlled evolution. This positive feedback closes the loop of Evolutional Intelligent Design, shortening its cycle time from billions of years to now billionth of a second.

If you are too busy to read this six-page Foreword on some of the 'ancient' histories that have occurred in less than ~ 30 years, which are the evidences of the inseparable tie between "evolution" and "intelligent design", then you should just skip forward to the book author's Preface and his Chapter 1, and then the rest of his book.

As you read this book, you will realize that it is such a complicated object, much more than the simple two-word acronym, EM. When finished, you will agree that it is an engineering masterpiece of eloquent, concise and succinct descriptions of a most important but also most engineering-complex subject. The invited young author, who has had decades of hands-on basic research and manufacturing experiences on this subject of Electromigration — EM, is Associate Professor Cher Ming Tan, presently with the Nanyang Technological University of Singapore.

This monograph is the fifth book in this series on modeling of integrated-circuit devices. Its purpose is to provide archival references, described by the model originators or authorities, on the devices and components that are to be integrated on a small, a centimeter or smaller, silicon semiconductor integrated circuit chip. It has been my intention to invite the experts to cover all the components of an integrated circuit. These include the active devices (MOS field-effect and bipolar-junction transistors), the passive devices (diodes, resistors, capacitors, and inductors), and the sensors that interface the electronics with the ambient and the user (electromagnetic

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and optical radiators and receivers or the antennas, biological sensors of ambient forces – pressures, flow velocities, accelerations). Not the least, we want to include the new electrical and mechanical devices when proven in applications and manufacturability. Certainly, the most important we must cover is the interconnects which are the metal conductor wires and plugs or studs, that electrically interconnect the devices and sensors, and the endurances of the interconnects during operation and shelve lives, which are the subjects of this book.

The monograph series idea came about when I was looking into the literature for references to write the keynote address. It was on the history of MOS transistor compact modeling. I was invited by the Founder of the Workshop on Compact Modeling, Associate Professor Xing Zhou of Nanyang Technology University and his international workshop program committee. It was the workshop's first keynote and it was to be presented at its fourth annual Workshop on May 10, 2005. A second purpose of this device-modeling monograph series was to provide state-of-the-art textbooks for graduate students and reference books for practicing engineers. These books would rapidly disseminate the detailed design methodologies and underlying physics, which are progressing at an ever faster rate, in the computer-aided-design of silicon semiconductor integrated circuits which contain hundreds, thousands, now billions, approaching if not already exceeding a trillion of diodes, transistors and interconnects on one small (< ~1 square centimeter) silicon die or silicon integrated circuit chip. It is also the objective of this monograph series to provide timely updates, via website and internet exchanges between the readers and authors, for immediate public dissemination, and to provide new editions when sufficient materials are accumulated.

I am especially thankful to the invited authors of the four startup volumes (Narain, Carlos+Márco, Mitiko+Hans+Tatsuya, and Arjun), and the invited authors of the later volumes (Cherming of this volume, Chenming+Weidong, Chinghsiang, Michael, Jamal, and others.). They concurred with my objectives and agreed to take up the chore of writing their books during their very busy schedules. Some have delays of one, two or even three years. Nevertheless, their monographs are still the archival records of the state of the art, and the world's authoritative contributions to the device modeling literature, because these authors are the creators and/or authorities of the models, and because the models are the industry-wide consensus models used by all circuit designers in the past and recent generations of integrated circuit designs.

The present volume is a review of the literature on Electromigration (EM) in metals. EM is the ultimate failure cause of silicon integrated circuits. It also affects, if not directly determines, the ultimate performance limit of silicon integrated circuits because the RC signal delay in digital switching circuits and resonance broadening and gain lowering in analog circuits are limited by the resistance of the metal interconnect line, R. This resistance increases due to EM, caused by the high density of electrical current through the interconnect lines. On the microscopic events leading to failure, in one failure mode, EM of the metal atoms of the metal conductor line leaves behind a void in the line, which eventually opens the line when the void grows to the cross-sectional area of the line, causing the transistors and devices to disconnect electrically. In the second mode of EM failure, the migrating metal atoms of the metal line can pile up at favored locations in the line. (Read this book to find where these favored locations are.) The pile-up of the metal atoms would grow to a sufficient size to electrically short-circuit the adjacent lines. Such shorts become increasingly frequent with increasingly closer adjacent lines as the circuit dimension, hence interline spacing, or the pitch, continually decreases into the nanometer range.

The vast engineering literature on EM is a reflection of the many chemical elements and

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compounds that make up the interconnecting metal lines and studs. The chemical composition is complicated further by the recent adoption of copper for its higher conductivity, in place of aluminum, to give lower R and RC delay, and to give higher signal amplification and Q or sharper pass band from RCL resonators for lower crosstalk and distortion. The complication in Cu interconnect structure arises because Cu diffuses easily into silicon to short out the devices. This must be prevented by diffusion barriers made of multi-layers of very thin films of buffer metal elements and compounds, and insulators. Additional complications come from the three-dimensional (3-D) geometries of the interconnection metal lines. All of these increase fabrication complexity and cost, and lower manufacturing yield.

For example, the 3-D interconnects (lines and studs through via's) are built into many (~10) levels over the thin silicon surface layer which contains the many silicon transistors, diodes, resistors and capacitors. **Planarization** (2-D) of each interconnects' layer is necessary to provide direct routing, in order to reduce the electrical signal delay in digital circuits through the length of interconnect metal lines. The transistors, at each of the technology generations, from micrometer to now nanometer, have always been much faster than the interconnects' RC delays. The 2-D planarization is also necessary to minimize abrupt changes in line directions, which could increase the electrical current density at the abrupt bends. The higher density would accelerate the rate of EM failure via void growth and metal pileup, directly via the microscopic interaction of the higher electric field at the bends with the migrating atom, and indirectly via space-gradients of atomic concentration (diffusion rate) or atomic flux divergence, and also space-gradients of the local lattice temperature (reaction or atomic trapping and detrapping rates). However, the chemical-mechanical polishing (CMP) or planarization technique is not only process tedious, but also a source of minute-impurity-incorporation and atomic damage or crystal defect formation from the bulk-penetrating surface roughing during the polishing step.

Furthermore, because of the many parameters that control EM, its engineering has been a factory art of recipe-driven, statistically optimized, empirical or trial-and-error task, influenced by the traditional chemical and metallurgical engineering practices of statistical control. This reminds me of a similar if not more well-known but certainly fully played-out case in a modern silicon integrated circuit factory. It is the person-specific favored fit-formula approach in modeling the dependence of the electron and hole mobility's on the concentration of the randomly located bulk and surface-interface impurities and defects, which scatter the electrons and holes, and on the local temperature and local electric field. It has been a subject of domain ownership by the manufacturing departments and individual engineers whose jobs and survivals are at stake. But, electron and hole mobility's are fundamentally and practically much simpler because they are electronic and **ma**croscopic even when the dimensions are now down to the **mi**croscopic nanometers, because there are still enough number of the interacting particles (electrons, holes and scattering centers) to allow a macroscopic modeling of the electron and hole mobility's. On the other hand, EM and the general phenomena of atomic migration under concentration and temperature gradients and under electric fields are much more complicated, because, they are atomic and **mi**croscopic even at the larger dimensions of the micrometer or micron era of yesteryears. This is further compounded now by the increasingly smaller dimensions into nanometers, resulting in even fewer atoms (and particles) responsible for EM. Worse, the traditional chemical-electrical-metallurgical engineers' empirical practice of thermally activated rate, given by the product of a jump or collision-frequency factor (frequently called the pre-exponential factor) and the Boltzmann factor $\exp(-E_{act}/kT)$ from the particle number variation

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with particle kinetic energy of a dilute concentration of scattering and scattered particles, was used by Black to fit the EM failure-time data, but its derivation has been based on a fundamentally flawed assumption of the presence of a Coulomb-like electrostatic force between the metal electrons and the metal ions, known as the electron wind force, like the rapidly moving and electrically neutral air molecules at rather dilute concentrations, that move a person, a tree, a building by the wind force. But, it ignored the fact that there are so many mobile conduction electrons in a metal, not unlike a glueish jello or an extremely high concentration of molecules in dense liquids, which could "instantaneously" "screen" the electrostatic force from the positively charged ionic core of each of the many metal atoms, preventing the charged atomic cores from "feeling" the negatively charged drifting electrons that carry the electrical current, rendering the electron-ion or electron-wind force untenable. The simple Debye screening length analysis shows that the many valence electrons in a metal (~ 10^{23} cm^{-3}) would screen the atomic ion charge in ~ 0.1A, which is much less than the inter-ion-core distance of the metal's lattice, ~ 2A, estimated from the inter-atomic core spacing or the lattice constant of the metal crystal.

As a consequence of the ppEM (pp=personal property), I was strongly discouraged by the "technology czar" of the world's leading silicon IC chip manufacturer, who happens to be also the most supportive to his former teacher among my 50 PhD students, to not enter this pp arena in 1980, because he just received a request to godfather the dispute, with a 3-foot pile of reports and stacks of 8-inch EM-test-pattern wafers. He told me that he would definitely be not able to loan me any 8-inch silicon wafers with interconnect patterns designed for EM tests since he had no ownership, unlike the generations of gate oxides (100A to 10A) and CMP silicon surfaces to investigate the interface traps on oxidized CMP silicon surfaces, for which (the CMP technology) he was the first to put into volume manufacturing for the semiconductor industry.

This EM episode has now triggered my memory on the history of these two dominating technologies (gate oxide and CMP) since EM is tightly coupled to both. It must be told since probably no one could except the actor himself who is too modest. This history also leads to the importance of CMP and hence its development with great efforts and best brains, and at substantial costs, asides from its secrecy, as a proven example of <u>intelligently designed evolution</u> with the characteristic time of about two years rather than the random Darwin evolution of millenniums or millionniums. There are two aspects, the manufacturing and the physics.

Let me first tell the story of EM manufacturing technology history. The CMP and gate oxide technologies were actually originated and <u>evolved</u> from the young-Shockley led group at Bell Telephone Laboratories (where else?) when the older Bardeen and Brattain of the group <u>discovered</u> the transistor "effects" in 1948 using the two point-contacts on chemically etched surface of a germanium single crystal called the 'bulk' to give the 3-terminal device that has the minimum number of leads or terminals necessary to give amplification of electrical signal. However, the point-contact transistor (PCT) of Bardeen and Brattain was plagued by instability and irreproducibility from the surface chemical treatments and even the exposure to ambient during and before operation. Such sensitivity and irreproducibility quickly closed the human's first transistor factory (Western Electric, 555 Union Boulevard, Allentown, Pennsylvania). I was lucky to see this world's first mechanically automated transistor factory, during my 1956 and first job interview before it was to close. So, Shockley <u>invented</u> (or "designed" via intelligence from prior learning and training) the two transistors to avoid surface effects, in 1952, the field-effect transistor (majority carrier drift current in the <u>bulk</u> of a semiconductor) and in 1949, the p/n junction transistor (minority carrier diffusion current also in the <u>bulk</u> of a semiconductor). We are

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still using these two transistors and their principles to this day, 60 years later. He, Shockley, designed their geometries to place the current path inside the semiconductor bulk, away from the semiconductor surfaces, to avoid the surface "effects" observed by Bardeen and Brattain in their PCT. However, the 3-D bulk device structures invented by Shockley evolved naturally to 2-D devices in a thin surface layer that is protected or passivated by a stable thermal silicon dioxide layer. Such 3-D to 2-D evolution was necessary to meet the demand of transistor operation not just for audio electronics (20-20K Hz) offered by the bulk transistors, but also at higher frequencies for the AM (550K to 1650K Hz) and FM (88M to 108M Hz) radios, and at still higher communication frequency bands, and also at higher speed for faster computer operations. The 3-D to 2-D evolution was also aimed to increase integration to put more electrical signal processing functions on one small silicon die (or chip). But fortunately (again an evolution by someone's design sometimes ago, billions of years ago) silicon is unique in having a surface oxide which is stable in the planet earth's ambient of oxygen and nitrogen, even some water vapor or hydrogen. No other chemical element's oxide has such electronic stability (tens of years or more) of one part per trillion change.

Thus, the historical path of the evolutionary invention of CMP as a practice of intelligent design, should not be surprising in its choice of routes and peoples, which I witnessed as part of the design and as the dispatch to tell its story: Shockley's BTL@1949 ➔ Shockley Transistor Corporation via Shockley@1956 ➔ Fairchild Semiconductor Corporation via Moore and Sah@1959 who previously both worked for Shockley ➔ UIUC (University of Illinois at Urbana-Champaign) via Sah@1962 ➔ Intel Corporation via Leo Yau who earned the PhD in ECE at UIUC under Sah in 1969, but delayed his arrival at Intel until 1977 via postdoctoral and junior faculty tenures ➔ USA and then world-wide semiconductor industry via Yau's Intel equipment contractor around ~1991. The Intel equipment contractor, found by Yau, was a German brother machine shop, which repeated the evolutional intelligent design cycle several times, with a period of about one year following Yau's designs. As the still going industrial practice today, it built the first ten units of the latest Yau design for Intel, then it was allowed to produce many more units of that same design for the rest of the semiconductor industry or Intel competitors for more profits at higher profit margins for the German brothers, while simultaneously producing for Intel the next generation from Yau's next design. Leo Yau escorted me through his 黄鼠狼窝 ("Shunk Works" = Yellow Rat Wolf Burrow), the Portland downtown riverfront German-brother machine shop, that was known to only a few Intel upper managers. To give me the private tour, they invoked the belief of the leak-proof teacher-student bond, in order to get a neutral witness from the academia. So, there is no doubt, at least in my mind, that the CMP technology for planarization of the interconnect lines and studs, that went into worldwide volume IC manufacturing in the 1990's, was an act of <u>evolution via intelligent design</u>. It had a total evolutional learning time of about 20 years (Yau's involvement time) or 40 years from Shockley Transistor Corporation's production in 1956 to reach volume manufacturing in ~1995 with about 10 technological increasingly more complex silicon transistor fabrication processing steps, initially bipolar then MOS integrated circuits, cumulated by Leo Yau's 黄鼠狼窝 at the Portland downtown river front. Their transition events or laboratory-jumping times are 1949-1956-1959-1962-1975-1995. No other self-proclaimed or company-designated inventors could possibly claim first or claim the CMP invention credit, regardless of their patent filing and issuing dates. Some companies, like Intel, reported by the media, do not file patent protection, relying solely on the trade-secret lead-time, since patent disclosures and claims hasten reverse engineering.

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Let us next turn to the fundamental EM physics, which is a story of how I got into this topic. I had hoped to take the opportunity in 1984 when a America-born and Nanjing-China educated Materials Science graduate student sought me out to work on a PhD thesis project, even for free if I could not come up with a paid research assistantship, by continuing washing dishes at the student cafeteria at UIUC. But how could I not, for one who had ranked first in all the graduate ECE classes she had to take to make up the deficiencies due to the transfer of major from Materials Science to Electrical and Computer Engineering. Therefore, I took this up as an "intelligent design" opportunity to look into the alternatives for the fundamentally flawed Black EM formula based on the electron-wind force, which I learned from reading Rolf William Landauer's 1956-1978 articles which led him to conclude the nonexistence of the electron-wind force even using the most basic fundamental formulation of the many-body problem. The alternative theory, which I then derived, was an electron-windless formula for neutral atoms moving away from a void in the metal line, causing the growth of the void. My simple kinetics formula was based on just diffusion and trapping and detrapping of neutral atoms on the surfaces and in the surface layer of a void, with no drift current and no ions. It was a very familiar subject to me, because I was drilled by Shockley 20 years earlier via all the theoretical analyses on the electron-hole generation-recombination-trapping statistics (kinetics), which had resulted in the 1958 Sah-Shockley Physics Review article. That was the second, and last I wrote under Shockley's tutelage. However, the 1984 pp that encircled Yau, derailed my hope, from not able to get industrial wafers with EM test patterns from Leo Yau at Intel to get the experimental proof of the windless theory.

Then, another 20 years later (~1984 to 2006), one more "intelligence design" appeared. I jumped at the window of opportunity. This happened when I was invited by Professor Kok-Khoo Phua (the second time, since he also invited me to start a book series with his book publishing company, the World Scientific Publishing Company, 15 years earlier in 1991, which is now publishing this EM book) to lecture and consult during November-December 2006 at the Nanyang Technological University (NTU) in Singapore. During the one-week on-site consulting review about NTU's teaching and research programs, I met a young associate professor, Cher Ming Tan. He rang my bell when he reported his EM work to the research review committee. Upon being asked by me during the meeting and the post-meeting one-on-one discussion, he showed and gave me a copy of his 250-page review article on EM, which was about to be published by the leading international journal on materials. I immediately invited him to write a book. He agreed. The rest is history, recorded and proven by this monograph.

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