Chapter 1

Introduction

Single-electron devices provide a means to precisely control the charging of a small conducting region at the level of one electron. These devices operate using the Coulomb blockade or single-electron charging effect (Devoret and Grabert, 1992; Likharev, 1999), where the energy associated with the addition or subtraction of one electron from a nanometre-scale electrode controls the electrical characteristics of the device. In comparison with conventional semiconductor devices, single-electron devices such as the single-electron transistor (SET) (Fulton and Dolan, 1987) and the single-electron memory cell (Nakazato *et al.*, 1993) are inherently nanometre-scale and highly scalable. Furthermore, these devices possess the advantages of ultra-low power consumption, associated with the very small amounts of charge they use, and immunity from statistical fluctuations in the charge (Nakazato *et al.*, 1993; Yano *et al.*, 1999). This has led to great interest in these devices for future LSI circuit applications.

Since the 1970s, the speed and performance of LSI circuits has improved dramatically, associated with a continuous reduction in the size of semiconductor devices. The minimum feature size in an integrated circuit has reduced from >1 μm in 1970 to ~50 nm in 2008, and it is expected that by 2011, it may be possible to define features smaller than ~20 nm (International Technology Roadmap for Semiconductors, 2007). At present, the physical gate length in high-performance metal-oxide semiconductor field-effect transistors (MOSFETs) may be as small as ~35 nm (Mistry *et al.*, 2007). At least with respect to the channel length, we may regard LSI MOSFETs as *nanoscale* devices, i.e. with dimensions in the range 1–100 nm.

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Conventional LSI circuit devices such as the silicon MOSFET, dynamic random access memory (DRAM) cells, and FLASH memory cells, operate using 'bits' defined by large numbers of electrons. For example, a DRAM cell uses ~100,000 electrons to define the '1' bit (Yano *et al.*, 1999). Similarly, silicon MOSFETs operate with large numbers of electrons, each electron behaving simply as a carrier of charge. We may therefore regard conventional LSI device operation as 'classical' and simply approximate the influence of quantum mechanical effects. Quantum mechanical effects in a heavily-scaled MOSFET include the gate leakage current associated with the tunnelling of electrons across thin gate oxide layers, corrections to the threshold voltage caused by energy quantization in the potential well of the inversion layer, and the possibility that a fraction of the channel current is associated with the ballistic transport of electrons (Taur and Ning, 1998).

With the reduction in MOSFET size deep into the nanoscale, short-channel effects (SCE) associated with the breakdown of the long-channel approximation in a MOSFET lead to an increase in the device current and a reduction in the threshold voltage (Taur and Ning, 1998). The increasing significance of SCE with reduced device size leads to the degradation of gate control over the channel current, an increase in the device 'off' current, and an increase in the static power consumption. This problem is most serious for high-speed devices, where the channel length is scaled most heavily. In high performance, sub-50 nm channel length MOSFETs, the drain source 'off' current $I_{sd,leak}$ is already ~30 nA/µm (ITRS, 2007). It is expected that, if the channel length reduces to ~10 nm by 2013, $I_{sd,leak}$ will increase to ~100 nA/µm or greater. The situation is somewhat better for larger (65 nm channel length), lower speed, low operating power MOSFETs, where $I_{sd,leak}$ ~1 nA/µm. However, this is also expected to increase, reaching ~10 nA/µm by 2013 (16 nm channel length). For even larger, low standby power devices, at present $I_{sd,leak}$ ~10 pA/µm (75 nm channel length) and is expected to increase to ~100 pA/µm by 2013 (18 nm channel length). The increase in $I_{sd,leak}$ complicates and may even limit device scaling, especially for high performance devices. Even in the best

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case, it is likely that complex system-level solutions may be needed to limit excessive power consumption (ITRS, 2007).

Other issues also arise as device size reduces into the nanoscale. Process tolerances may lead to variations in the structure of nominally identical devices, e.g. variations in gate-oxide thickness or channel length. These effects cause greater variation in the characteristics of a nanoscale device. Furthermore, charge fluctuations between different devices, e.g. changes in the charge in the channel or fluctuations in the doping concentration in nominally similar devices, become increasingly significant and may lead to variation in the electrical characteristics between different devices (Ferry and Goodnick, 1997). As an example, a nanoscale region 10 nm × 50 nm × 1 μm in size, doped *n*-type at a concentration of $10^{17}/cm^3$, would possess on average only 5 dopant atoms. Statistical '$\sqrt{n}$' variations in this number of dopant atoms are clearly unacceptable, and higher doping levels would be needed.

Since the 1980s, the ability to fabricate nanoscale devices has led to a large body of work on novel semiconductor devices directly using quantum mechanical effects for their operation (Ferry and Goodnick, 1997). These include *quantum dots* in vertical and planar III-V heterostructure material (Reed *et al.*, 1988; Kouwenhoven *et al.*, 1991), where quantum confinement of electrons in a potential well in one or more dimensions influences the electrical characteristics, ballistic transport devices such as quantum point-contacts (van Wees *et al.*, 1988, Wharam *et al.*, 1988), and single-electron devices. The latter allow control over charge at the level of *one* electron. Initially, the great interest in these devices was driven by investigations of *mesoscopic* physics, i.e. the physics of structures larger than the atomic scale, but smaller than the macroscopic scale, where Boltzmann transport theory would apply (Ferry and Goodnick, 1997).

Early, relatively large (~100 nm) quantum effect devices required cryogenic temperatures to work. While this is not an issue for experiments investigating the physics in these devices, clearly it prevents the practical application of such a device in most cases. However, the potential of single-electron devices such as the SET, and the single-electron 'box' for integrated circuit applications was identified even in the earliest investigations (Likharev, 1988). Clearly, if charge storage on

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a nanostructure could be controlled at the one electron level, then the number of electrons necessary to define a single bit could be dramatically reduced, leading to a large reduction in the power consumption of the device (Yano *et al.*, 1999). Control of charge at the one electron level would also eliminate any statistical, '$\sqrt{n}$' variations in the electron number n, removing the effect of these variations in large numbers of devices (Nakazato *et al.*, 1993). Furthermore, if a quantum device was fabricated using conventional LSI-compatible materials and fabrication techniques, e.g. if the device was fabricated in silicon, then LSI fabrication technology would be available for the circuit integration of the device. In addition, quantum devices often operate at very small current levels. Amplification of these levels would then be necessary for interfacing with other electronic devices, on or off a chip. Compatibility with conventional LSI technology implies that MOSFETs could be used to provide this interface, allowing quantum devices to communicate with the 'outside world'.

Devices operating using quantum mechanical principles can often *improve* in performance with reduction in device size (Yano *et al.*, 1999). For example, in a single-electron device, a reduction in the size of the device to ~10 nm leads to an increase in the maximum operating temperature of the device to room temperature (Takahashi *et al.*, 1995). Similarly, the energy level separation in a quantum dot increases with a reduction in the dot size (Saitoh and Hiramoto, 2002). Furthermore, the voltage levels in these devices also increase, to values closer to those used in conventional MOSFETs. In contrast, MOSFETs become increasingly complex in structure as the device size is reduced and effects such as SCE or tunnelling across the gate oxide tend to degrade the electrical characteristics. The development of practical single-electron devices allows us to envisage low power, highly integrated circuits using devices only ~10 nm in scale, operating with ultra-small charge packets containing, at most, a few electrons.

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1.1 Single-Electron Effects

Single-electron charging effects provide a means to control the charge on a small, nanometre-scale conducting region at the level of one electron (Devoret and Grabert, 1992; Likharev, 1999). Consider a conducting region fabricated in either a metal or a doped semiconductor, with dimensions ~100 nm or less. The size of this region is such that it forms a *nanostructure*. Furthermore, consider that the conducting region, or *island*, is near two other conducting regions, or electrodes, and that an insulating material lies in the gaps (Fig. 1.1[a]). If the widths of the gaps are small, each ~10 nm or less, then a voltage difference applied across the electrodes can transfer electrons on to, and off the island by quantum mechanical tunnelling. The gaps then form tunnel barriers, with an associated energy barrier (Fig. 1.1[b]). Such a system is called a single-island, double tunnel junction.

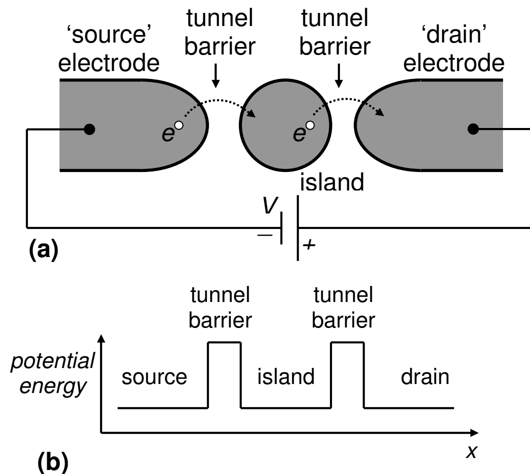

Fig. 1.1 The single-island, double tunnel junction system. (a) Schematic diagram, where the island and electrode regions (shaded) are formed by conducting materials. The gaps between these regions form tunnel barriers. (b) The potential energy across the system, at zero bias.

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Electrons can tunnel onto the island only if the charging energy associated with adding the electrons to the island is overcome (Devoret and Grabert, 1992). If the total capacitance of the island is C, then the charging energy of a *single* electron added to the island is given by $E_c = e^2/2C$. This is referred to as the *single-electron charging energy*. It is essential that this energy is overcome before an electron can tunnel onto the island. With a nanometre-scale island ~100 nm or less in size, it is easily possible that $C \sim 10^{-16}$ F or less (Fulton and Dolan, 1987). This implies that the single-electron charging energy $E_c \geq 0.8$ meV. At cryogenic temperatures, e.g. at the temperature of liquid Helium, $T = 4.2$ K, the thermal energy $k_BT = 0.36$ meV, where k_B is Boltzmann's constant. We therefore have a system where $E_c > k_BT$ and the thermal energy may not be enough to allow an electron to tunnel onto the island. If we were to reduce the island size further, reducing C and increasing E_c, then E_c may be $\gg k_BT$ and the likelihood of an electron tunnelling onto the island because of the thermal energy it possesses becomes very small. If $C \sim 10^{-18}$ F, a possibility if the island size is ~10 nm (Takahashi *et al.*, 1995), then $E_c \sim 80$ meV, greater than $k_BT = 26$ meV at room temperature, $T = 300$ K. This implies that, even at room temperature, the thermal energy is insufficient for an electron to tunnel onto the island.

Assuming that $E_c \gg k_BT$, we now attempt to transfer electrons onto the island by applying a voltage V_{ds} across the two electrodes. We shall now refer to the electrodes as the drain and source electrodes, a bias being applied to the drain electrode and the source electrode being considered as 'ground'. The circuit diagram of the system is shown in Fig. 1.2(a). Here, the tunnel junctions have capacitances C_1 and C_2, and resistances R_1 and R_2, and the total island capacitance is $C = C_1 + C_2$. The voltage V_{ds} creates a potential difference between the intermediate island and each of the electrodes. For a small positive value of V_{ds}, the potential difference V_1 between the higher energy, source electrode and the island is small enough such that $E_c = e^2/2C$ is not overcome. Therefore, electrons on this electrode cannot tunnel onto the island. However, if V_{ds} is increased such that E_c is overcome, an electron can tunnel onto the island. This electron can then tunnel off the island to the lower energy, positively biased drain electrode, and a current begins to flow across the system. A further electron can then tunnel immediately onto the island,

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repeating the process. On average, the island charge increases by one electron. In a similar manner, for negative values of V_{ds} large enough such that potential difference between the drain and the island is large enough to overcome E_c, electrons can tunnel from the drain to the source, with current flowing in the opposite direction. For low values of V_{ds}, electrons cannot overcome the single-electron charging energy and cannot tunnel onto the island, and a current cannot flow. This is called the *Coulomb blockade* effect, and leads to the *I-V* characteristics shown in Fig. 1.2(b). Ideally, at 0 K, a zero current region or *Coulomb gap* exists for $|V_{ds}| < |V_c|$, where V_c is the *Coulomb blockade voltage*. At small finite temperatures, a small thermally activated current exists within the Coulomb gap.

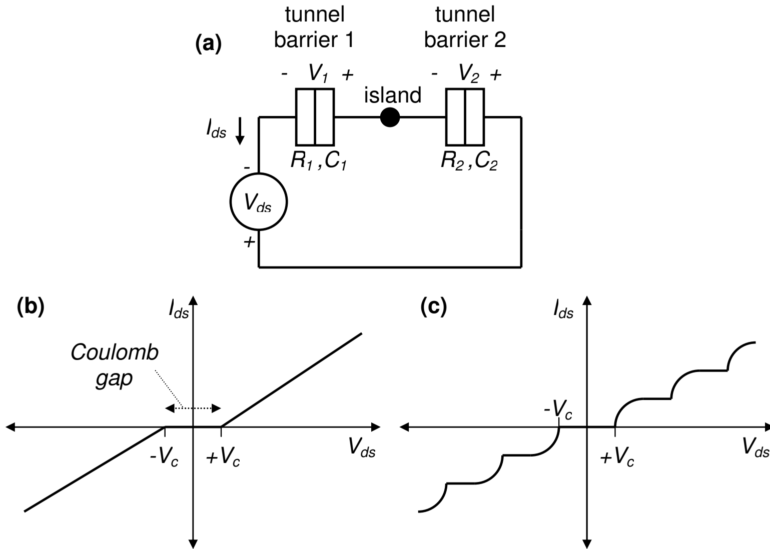

Fig. 1.2 (a) Circuit diagram of the single-island, double tunnel junction system. (b) Coulomb blockade *I-V* characteristics. If the tunnel barriers are similar, the current increases in magnitude linearly outside the Coulomb gap. (c) Coulomb staircase *I-V* characteristics. If the tunnel barriers are very dissimilar, the current increases in magnitude in a stepwise manner.

We now increase V_{ds} beyond the Coulomb gap edge $+V_c$. When V_{ds} reaches a value such that the charging energy corresponding to two

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electrons $2E_c = e^2/C$ is overcome, a second electron can persist on the island, and on average, two extra electrons exist on the island. With further increases in V_{ds}, the number of electrons charging the island increases one-by-one. If the tunnelling rates across the two tunnel junctions are similar, the current increases linearly outside the Coulomb gap. However, if the tunnelling rates are very different, then the current rises in a non-linear, stepwise manner, creating a *Coulomb staircase* in the *I-V* characteristic (Fig. 1.2[c]). Each successive step in the characteristics corresponds to an increase in the number of electrons on the island by one.

A further restriction on single-electron charging effects is imposed by the nature of the tunnel barriers that quasi-isolate the island. If the tunnel barriers are too conductive then charging electrons cannot be localized on the island. Quantum mechanically, for single-electron charging to occur, the electron wavefunction must not extend strongly across the tunnel barriers into the electrodes. Localization of electrons on the island is possible if the tunnel barrier resistance R_t is greater than the resistance quantum $R_k = h/e^2 \approx 25.8$ kΩ, where h is Plank's constant, i.e. $R_t >> R_k$ (Devoret and Grabert, 1992). In practice, this usually requires that R_t is at least ~$10R_k$. Furthermore, it is necessary for the tunnel barrier height $E_t >> k_BT$, in order to prevent thermally activated current over the potential barrier. The relatively large value of R_t in single-electron devices implies that these are high resistance devices in comparison with MOSFETs.

1.2 Early Observations of Single-Electron Effects

The possibility that the single-electron charging energy of a nanoscale island influences subsequent tunnelling events to the island was identified as early as the 1950s. In 1951, C.J. Gorter proposed that the observed increase in resistance of thin, granular metal films at low electric field and temperature was associated with the need to overcome the energy required to transfer an electron from one grain to another (Gorter, 1951). Figure 1.3(a) shows a scanning electron micrograph of a thin metal film of Au, nominally ~5 nm thick, evaporated on GaAs. The film is strongly granular in nature, with a range of grain sizes. The

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smallest grains are only ~10 nm, small enough for significant single-electron charging effects. In further measurements, Neugebauer and Webb (Neugebauer and Webb, 1962) explained the in-plane conductivity of various granular metal films with grains ~1 – 10 nm in size, at low temperature down to 77 K, using a model where electron transfer between the grains was determined by an activation energy associated with the single-electron charging energy.

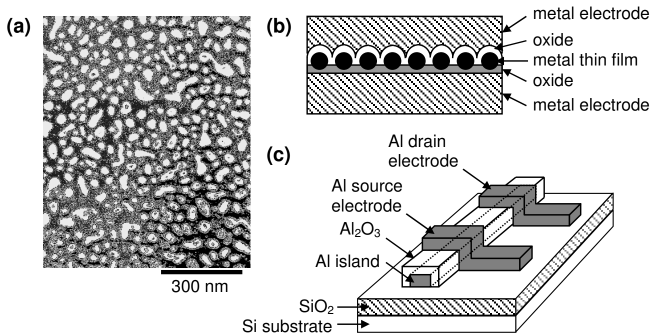

Fig. 1.3 (a) Scanning electron microscope (SEM) image of a granular Au film, average thickness 5 nm, evaporated on a GaAs substrate. Single-electron effects can be observed in the in-plane conduction through such a film, associated with the Au nanoparticles. (b) Metal electrode/oxide/granular metal film/oxide/metal electrode structure. Single-electron effects caused by the nanoparticles in the granular metal film can be observed in *I*-*V* or *C*-*V* characteristics measured across the two electrodes. (c) The Al/Al_2O_3 single-electron transistor, demonstrated by Fulton and Dolan in 1987.

These early works were extended by measurements of single-electron charging in thin metal films sandwiched between top and bottom contacts. Figure 1.3(b) shows a schematic diagram of such a structure. A thin oxide layer is grown or sputtered onto a metal contact. This is followed by the evaporation of a thin metal film on top, forming a layer of metal nanoparticles. A thin oxide layer is then grown or sputtered on top of the granular metal film, and finally a metal contact is deposited on top. The thin oxide layers form tunnel barriers for *I*-*V* measurements across the structure. Alternatively, one of the oxide layers can be thicker, forming a capacitor. *C*-*V* measurements can be performed on such a

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structure, where electrons are transferred into the metal nanoparticles only across the thinner oxide layer by tunnelling. Giaever and Zeller, in measurements of tin nanoparticle films embedded within an insulating matrix, observed an increase in the film resistance at low voltages in both normal and superconducting mode, at temperatures down to 1.6 K (Giaever and Zeller, 1968; Zeller and Giaever, 1969). This was explained by considering the charging energy of a single electron on a nanoparticle. Lambe and Jaklavic (Lambe and Jaklavic, 1969), in *C-V* measurements at 4.2 K on capacitors formed by metal nanoparticles (a system very similar to the 'single-electron box' described in the next section), observed charge quantization on the nanoparticles. These works, and further quantitative analysis by Kulik and Shekhter (Kulik and Shekhter, 1975), led to a good understanding of single-electron effects in granular metal films by the 1970s. By the mid-1980s, Likharev and co-workers (Likharev and Zorin, 1985; Averin and Likharev, 1986) predicted theoretically in great detail the behaviour of a single nanoscale tunnel junction. This was followed by the observation of a Coulomb staircase in the *I-V*, and differential resistance *dI/dV* vs. *V*, characteristics of granular films with well-defined tunnel barriers (Kuzmin and Likharev, 1987; Barner and Ruggiero, 1987). These characteristics corresponded to the addition of electrons one-by-one onto the island of a double tunnel junction.

In the preceding experiments, the island was defined 'naturally' by the granular nature of a thin metal film. By the late 1980s, advances in nanofabrication techniques implied that it was possible to fabricate well-defined nanoscale islands and tunnel junctions. This led to the demonstration of the first SET, by Fulton and Dolan (Fulton and Dolan, 1987), with a Coulomb gap in the *I-V* characteristics, and oscillations in the Coulomb gap with gate voltage. Figure 1.3(c) shows a schematic diagram of an Al/Al_2O_3 SET, formed on a SiO_2 on Si substrate. The island is formed by an aluminium electrode, and aluminium oxide tunnel barriers are formed by oxidizing the island. Two further aluminium electrodes, deposited across the island, form source and drain contacts. The silicon substrate may be used as a gate electrode, coupled capacitively to the island. In the device of Fulton and Dolan, the island electrode was formed by a ~14 nm thick Al layer, with dimensions

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~800 nm × 50 nm. The total island capacitance C ~ 1 fF and E_c ~ 100 μV, requiring measurements at milli-Kevin temperatures such that $E_c >> k_BT$. The Coulomb gap in the device was ~1 mV.

It is possible to fabricate well-defined islands and tunnel barriers in the Al-Al_2O_3 system, and this system is widely used for metal single-electron devices. However, these devices typically operate at cryogenic temperatures, and raising the maximum temperature of single-electron effects requires far smaller islands. In the first observation of a Coulomb staircase at room temperature, Schönenberger *et al.* (Schönenberger *et al.*, 1992) used a scanning tunnelling microscope to characterize a thin granular metal film with islands only ~1 nm size. Furthermore, even in the early stages of single-electron research, a large number of applications of single-electron devices, from quantum metrology, to sensitive electrometers, to transistors, memory and logic devices for integrated circuit applications, were identified (Likharev, 1988).

Single-electron effects in a semiconductor system were first observed in the conductance of a one-dimensional (1-D) channel of a silicon MOSFET at low temperature (Scott-Thomas *et al.*, 1988, and the follow-up paper by Van Houten and Beenaker, 1989). Here, disorder in the channel potential isolated a segment of the channel between tunnel barriers, forming an island for single-electron charging. Small islands were also defined by lithography in the two-dimensional electron gas (2-DEG) layer in III-V heterostructures. In these devices, patterned surface gates were used to form the tunnel barriers, by depleting sections of the 2-DEG in AlGaAs/GaAs heterostructure material (Meirav *et al.*, 1990; Kouwenhoven *et al.*, 1991a). At low temperatures, quantum confinement effects occur simultaneously with single-electron effects in the island, forming a quantum dot.

A very large body of work now exists on quantum dots in 2-DEGs, driven by investigations of the physics of zero-dimensional systems (Kouwenhoven *et al.*, 1997). Single-electron devices may also be fabricated in silicon-on-insulator (SOI) material, by patterning the top silicon layer using high-resolution electron beam lithography and etching (Ali and Ahmed, 1994). This provides a very flexible means to fabricate single-electrons devices with nanoscale islands, e.g. the first SET operating at room temperature was fabricated by Takahashi *et al.*

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(Takahashi *et al.*, 1995) in SOI material using electron beam lithography and oxidation. Here, the island size was only ~10 nm, the island capacitance $C \sim 10^{-18}$ F and $E_c \sim 0.1$ V.

There are a number of detailed, general reviews of single-electron devices. Early work on the subject has been reviewed by various authors (Likharev, 1988; Averin and Likharev, 1991; Schön and Zaiken, 1990; Devoret *et al.*, 1992). The reader is also referred to the book *Single Charge Tunneling*, edited by Grabert and Devoret (Grabert and Devoret, 1992), covering the theoretical and experimental state-of-the-art in 1992 in great detail. There is a later general review by Likharev (Likharev, 1999). Semiconductor single-electron devices are reviewed by Meirav and Foxman (Meirav and Foxman, 1996) and devices in silicon by Takahashi *et al.* (Takahashi *et al.*, 2002). Quantum dots are reviewed by Ashori *et al.* (Ashori *et al.*, 1996), van Houten *et al.* (van Houten *et al.*, 1993), and Kouwenhoven *et al.* (Kouwenhoven *et al.*, 1997). Interacting or 'coupled' quantum dots are reviewed by van der Wiel *et al.* (van der Wiel *et al.*, 2002). There are also various special issues of journals, focusing on single-electron and quantum dot devices (special issues of Z. Physik, 1991; Physica B, 1993; IEICE Transactions on Electronics, 1998). Furthermore, there are reviews for the more general reader, by Likharev and Claeson (Likharev and Claeson, 1992) and by Harmans (Harmans, 1992). Finally, a general review of electron transport in nanostructures, including single-electron devices, is given by Ferry and Goodnick (Ferry and Goodnick, 1997).

1.3 Basic Single-Electron Devices

We now introduce three basic single-electron devices, the single-electron transistor (SET) (Fulton and Dolan, 1987), the single-electron box (Lafarge *et al.*, 1991) and the multiple-tunnel junction (MTJ) (Delsing, 1992; Nakazato *et al.*, 1992). These three devices form the most common single-electron systems, and are the basis of more complex single-electron circuits such as single-electron memory (e.g. Yano *et al.*, 1999; Irvine *et al.*, 2000), single-electron logic circuits (Tsukagoshi *et al.*, 1998) and single-electron electron transfer devices

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such as single-electron pumps and turnstiles (Geerligs *et al.*, 1990; Pothier *et al.*, 1991). Hybrid devices consisting of combinations of the three basic devices may also be fabricated, e.g. the MTJ/single-electron box hybrid (Nakazato *et al.*, 1993) can form a single-electron memory cell, a configuration which has been widely investigated.

1.3.1 Single-electron transistor

Adding a third 'gate' terminal, electrostatically coupled to the island of the simple double tunnel junction discussed earlier converts the system into an SET (Fulton and Dolan, 1987). The circuit diagram of the SET is shown in Fig. 1.4(a). Here, a capacitor C_g connects the island to the gate.

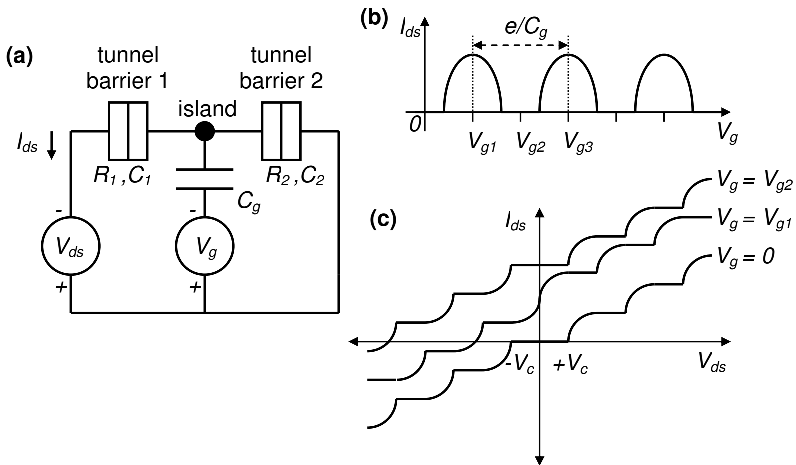

Fig. 1.4 (a) The SET. (b) Periodic single-electron oscillations in the I_{ds}-V_g characteristics, at a constant value of V_{ds}. (c) As V_g is varied, the edges of the Coulomb gap in the I_{ds}-V_{ds} characteristics vary periodically, e.g. from $\pm V_c$ at V_g = 0 V, to zero at $V_g = V_{g1}$, to $\pm V_c$ at $V_g = V_{g2}$. Here, for clarity, the three I_{ds}-V_{ds} characteristics are offset in I_{ds} from each other by equal amounts.

The gate voltage V_g may be used to control the Fermi level of the island, and overcome or impose a Coulomb blockade. This leads to the I_{ds}-V_{gs} characteristics shown schematically in Fig. 1.4(b), where at a constant value of V_{ds}, I_{ds} oscillates periodically. These characteristics,

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known as single-electron current oscillations, or Coulomb blockade oscillations, may be understood as follows. Applying a positive gate voltage V_g lowers the island Fermi energy, and at a value $V_g = V_{g1}$, the energy difference between the source and island caused by the single-electron charging energy is overcome. Electrons can then transfer from source to drain, across the island and a current is observed. We may view this as a reduction in the Coulomb gap to zero. Increasing V_{gs} lowers the island Fermi energy further. In Fig. 1.4(b), at $V_{gs} = V_{g2}$, the Coulomb blockade associated with a second electron on the island is yet to be overcome, and the current is very low. Increasing V_{gs} even further to V_{g3} overcomes the Coulomb blockade, and a second electron charges the island. Further increase in V_{gs} causes I_{ds} to oscillate periodically with a period e/C_g, each oscillation corresponding to a change in the electron number on the island by one. Furthermore, in the I_{ds}-V_{ds} characteristics (Fig. 1.4[c]), adjusting V_{gs} to a value corresponding to an oscillation peak leads to the Coulomb gap reducing to zero. Varying the gate voltage leads to a periodic oscillation in the Coulomb gap observed in the I_{ds}-V_{ds} characteristics. The SET can then be regarded as a simple switch, controlled by the gate voltage. For small values of V_{ds}, the SET is 'on' when the Coulomb blockade is zero and 'off' when a Coulomb blockade exists.

1.3.2 Single-electron box

Replacing one of the tunnel junctions of the single-island double tunnel junction by a capacitor forms the single-electron box (Lafarge *et al.*, 1991). The circuit diagram of the device is shown in Fig. 1.5(a), where the capacitor C_b replaces one of the tunnel junctions. C_b blocks DC current flow across the device, but charge may still be transferred onto or off the island from the source electrode, across the remaining tunnel junction. Applying a positive voltage V to the capacitor lowers the Fermi energy of the island relative to the Fermi energy of the source. When the Fermi energy of the island is lowered relative to the source by a value greater than the single-electron charging energy of the island, electrons can be transferred onto the island, charging C_b. Here, the single-electron energy is given by $E_c = e^2/2(C_1 + C_b)$. As before, it is

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necessary that $E_c > k_BT$, requiring that C_b is small. However, C_b must not behave as a tunnel capacitor, as electrons would then tunnel off the island. When the value of V_s is such that the Fermi energy difference between the source and the island just exceeds E_c, one electron transfers onto the island. As the Fermi energy difference exceeds $2E_c$, a second electron transfers onto the island and, in this way, electrons may be transferred onto the island one-by-one (Fig. 1.5[b]). Similarly, applying a negative voltage removes electrons from the island (assuming a metallic island) one-by-one.

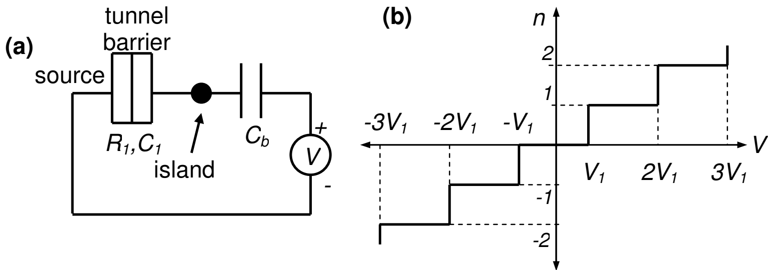

Fig. 1.5 (a) The single-electron box. (b) Electron number n on the island, as a function of applied voltage V.

We may contrast the single-electron box, where there is no DC current, with the double tunnel junction. In a double tunnel junction, it is also possible to charge the island with a precise number of electrons, but this is accompanied by a DC current across the device. The current is zero only within the Coulomb gap, when there are no extra electrons on the island.

1.3.3 Multiple-tunnel junction

The double tunnel junction and the single-electron box both contain only one island. It is also possible to observe single-electron charging effects with more than one island, connected to each other and to the electrodes by tunnel junctions. Such a system is referred to as a multiple-tunnel junction (MTJ) (Delsing, 1992; Nakazato *et al.*, 1992).

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Figure 1.6(a) shows the circuit diagram of an MTJ with *N* tunnel junctions, and *N*-1 islands. In such a system, a much larger Coulomb gap is often observed. This may be considered, to an approximation, to be determined by the sum of the single-electron charging energies of the constituent islands (Delsing, 1992). The MTJ may be used as the basis of an SET, with a gate electrode coupled electrostatically to one or more islands (Fig. 1.6[b]). Furthermore, an MTJ version of the single-electron box is also possible (Fig. 1.6[c]), where the tunnel junction is replaced by an MTJ. Here, charge is transferred onto the capacitor C_b across the MTJ, if the source voltage V_s has a negative value high enough to overcome the Coulomb blockade of the MTJ.

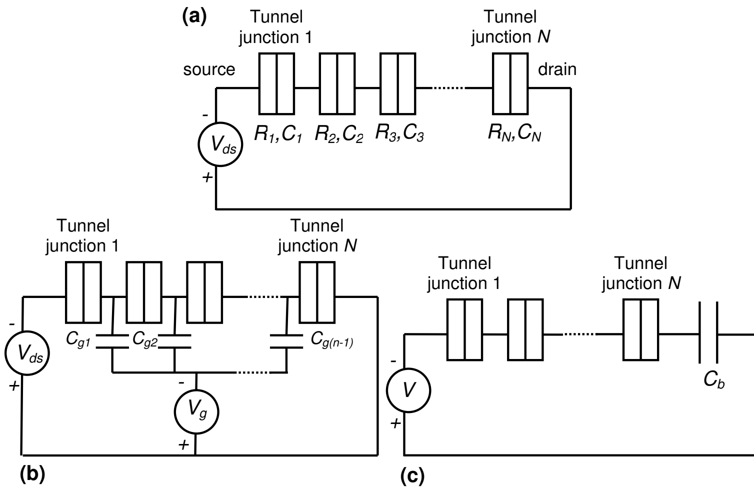

Fig. 1.6 (a) The MTJ. (b) The MTJ SET. (c) The MTJ single-electron box, or MTJ single-electron memory.

There are, however, significant differences between an electron box using an MTJ, and a simple single-electron box. Unlike a single-electron box, returning the source voltage V_s to zero after transferring electrons onto C_b does not remove the electrons charging C_b, as the MTJ remains within its Coulomb gap. A positive voltage is necessary to remove these electrons, leading to a 'memory' effect in the device. Furthermore, unless

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C_b is very small, it will hold multiple electrons. However, it is easily possible to fabricate an MTJ electron box that holds only a few electrons (Nakazato *et al.*, 1993), forming a few-electron memory cell. It is also possible to reduce C_b to a value similar to the MTJ tunnel capacitances, leading to a true 'single-electron' memory cell (Stone and Ahmed, 2000). We note, however, that in all these cases, electrons are controlled by an MTJ in Coulomb blockade, i.e. by single-electron effects (Yano *et al.*, 1999). The MTJ memory cell may therefore be referred to as a 'Coulomb blockade' memory cell (Durrani *et al.*, 2000).

1.4 Scope of This Book

This book discusses the design, fabrication and electrical characterization of single-electron devices and circuits in silicon. We discuss the physics of single-electron charging effects in detail, and provide an introduction to quantum dots. The book then discusses the fabrication and operation of nanoscale SETs in various silicon-based material systems. Single-electron memory devices are reviewed, where the stored 'bits' are defined by a few tens of electrons at most. We then consider few-electron charge transfer circuits such as single-electron pumps and turnstiles, where packets of charge consisting of one, or at most, a few electrons are transferred through a circuit using radio-frequency (r.f.) signals. Finally, the application of single-electron devices for logic operations is discussed.

We follow an approach where various single-electron device designs in silicon are reviewed, and examples from the author's research are used to illustrate the fabrication process and the electrical characteristics in detail. The book focuses on silicon single-electron devices as these are compatible with LSI fabrication techniques, and are of particular interest for the development of future, highly-scaled LSI circuits. A wide range of single-electron devices and circuits have now been demonstrated in the laboratory, often with LSI applications in mind. However, as we have seen earlier in this chapter, single-electron devices have been investigated equally widely in many other material systems, e.g. the Al/Al_2O_3 metal island system, or in AlGaAs/GaAs heterostructure

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materials. However, these devices are perhaps of greater interest for investigations of the physics of nanostructures than for LSI circuit applications. We therefore consider devices in systems other than silicon only occasionally, usually when they pre-date equivalent devices in silicon and understanding their operation is essential to a discussion of later devices in silicon. For more information on single-electron devices in other systems, the reader is referred to the list of general review papers provided earlier in this chapter.

1.4.1 Introduction to subsequent chapters

The subsequent chapters of this book are organised as follows. Chapter 2, 'Single-Electron Charging Effects', describes the theoretical basis of single-electron effects. After a brief introduction, the basic requirements for single-electron charging in a nanoscale system are discussed. The chapter then introduces single-electron effects in a single tunnel junction, and the observation of single-electron tunnelling oscillations in the current through the junction. These oscillations, at a frequency $f_{SET} = I/e$, provide a means to link frequency, current and charge at a fundamental level. The chapter then discusses the single-electron box. In this more practical device, energy fluctuations in the environment are decoupled from the charging island. For simplicity, the device is analysed assuming a metallic island. The change in the total electrostatic energy of the island, when electrons are added or removed from the island, is calculated first. This is then used to calculate the electron tunnelling rate. The concept of the 'critical charge' is discussed, the extent of the Coulomb blockade region in the device is defined, and an energy band picture for the device is introduced. The chapter then discusses the SET, again assuming a metallic island. The electrostatic energy changes and electron tunnelling rates in the basic double tunnel junction, and in the SET, are calculated. The tunnelling rates are then used to derive an expression for the *I-V* characteristics of the SET. The Coulomb staircase and single-electron current oscillations in the SET, the charge stability regions of the SET, the effect of nearby 'offset' charges, and energy band pictures are discussed. Finally, the chapter provides a brief introduction to quantum dots, where quantum confinement of

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electrons on the island leads to discrete energy levels on the island. These effects are of greater significance in devices where the island is defined using semiconductors. Our discussion considers the energy band diagram for a quantum dot, the 'addition energy' of the quantum dot, and the effect of quantum confinement effects on the electrical characteristics of the quantum dot.

Chapter 3, 'Single-Electron Transistors in Silicon', describes the design, fabrication and characterization of SETs in crystalline and nanocrystalline silicon material. The chapter begins with an introduction to early observations of single-electron effects in silicon, and the first silicon SET designs. The chapter then discusses SETs fabricated in crystalline silicon. SETs with lithographically defined islands are reviewed, including SETs fabricated in SOI material, with islands defined by etching and oxidization, room temperature SET designs and SETs based on MOSFET structures. Techniques such as pattern-dependant oxidation, used to define well-controlled islands ~10 nm in scale, are discussed. We then discuss SETs using silicon nanowires defined in SOI material. Here, fluctuations in the doping concentration, surface potential, etc. lead to the formation of MTJs along the nanowires. SETs with ultra-small islands ~5 nm or less in size, where room-temperature single-electron oscillations with high peak-to-valley ratios are observed, are introduced. The chapter then discusses the design, fabrication and characterization of a nanowire SET in SOI material, defined using electron-beam lithography. The electrical characteristics of the device, including room temperature operation, are discussed in detail.

The second part of the chapter discusses SETs in nanocrystalline silicon material, where the islands are defined 'naturally' by growth techniques rather than high-resolution lithography. The formation of potential barriers at the grain boundaries in nanocrystalline silicon thin films, and the conduction mechanism across such a film, are introduced first. This is then followed by a review of SETs in nanocrystalline silicon films, where the grains define islands and the grain boundaries define tunnel barriers. We discuss nanocrystalline silicon nanowire SETs, and scaling of these devices to form 'point-contact' SETs capable of room-temperature operation. We then discuss SETs where the islands are formed by discrete silicon nanocrystals. The observation of electrostatic

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and electron wavefunction coupling effects in nanocrystalline silicon SETs is considered. Finally, the chapter discusses single-electron effects in silicon nanowires and nanochains, synthesized by material growth processes rather than by lithographic techniques.

Chapter 4, 'Single-Electron Memory', discusses single-electron, and few-electron memory cells and circuits. In these devices, the Coulomb blockade effect is used to store information 'bits' consisting of single electrons or, at most, a few tens of electrons. The chapter begins with a brief historical introduction to charge storage in single-electron systems, and a discussion of the first single-electron memory design, the MTJ single-electron memory. Here, an MTJ is used to trap a small number of electrons on a memory node. The chapter discusses the concept of 'critical charge', and the hysteresis in the charge stored in the device. The chapter goes on to discuss MTJ memory designs in silicon, with various means to 'sense' the stored charge, e.g. using SETs or using scaled MOSFETs. A scaled MTJ memory cell, where one electron can be stored and sensed, is also discussed. This is followed by a brief review of single-electron memories using nanostructured 'floating gates' placed between insulating layers to store the charge. Here, the floating gate may be formed by a layer of silicon nanocrystals, or by a single, nanoscale floating gate. The silicon nanocrystals, or the scaled floating gate, may be small enough for room temperature single-electron effects. The chapter then discusses more complex memory designs, e.g. background charge insensitive single-electron memory, and a 128 Mb LSI single-electron memory in nanocrystalline silicon. Finally, the chapter discusses in detail the fabrication and characterization of an MTJ few-electron memory with MOSFET sensing, ~60 electrons per bit, and writing times ~10 ns.

Chapter 5, 'Few-Electron Transfer Devices', discusses the design, fabrication and operation of single-electron circuits capable of controlling the transfer of charge packets consisting of single electrons, or only a few electrons, using r.f. signals. The chapter begins with an introduction to the first single-electron transfer devices demonstrated, the single-electron turnstile and the single-electron pump. While these devices were implemented initially in the Al/AlO_x and the GaAs/AlGaAs 2-DEG system and not in silicon, the design of other electron transfer

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systems relies on the concepts developed by these devices. The chapter then considers silicon MTJ-based bi-directional electron pumps and turnstiles, which may be regarded as MTJ analogues of the basic single-electron pump and turnstile. However, the charge packets in these devices consist typically of a few electrons and not one electron. Various designs of MTJ-based electron pumps/turnstiles are possible, using one or more r.f. signal. The chapter then considers single-electron transfer in other types of devices, e.g. nanoscale charge-coupled devices, and hybrid designs using integrated SETs and MOSFETs. Finally, the chapter briefly discusses metrological applications of single-electron transfer circuits.

Chapter 6, 'Single-Electron Logic Circuits', discusses systems where single, or at most a few electrons, are used to perform logic operations. Single-electron logic is possible using two approaches. One approach uses SETs as switching transistors in a manner similar to conventional logic circuits, and is referred to as 'voltage state' logic. An alternative approach uses a single electron, or a few-electron packet, to represent a bit. The physical presence of the electron packet at a given point in the logic circuit then represents a '1', and the absence of the packet represents a '0'. This approach is referred to as 'charge state' logic. The chapter first considers devices operating using voltage state logic. These include SET analogues of *p* and *n* metal oxide semiconductor (*p*-MOS and *n*-MOS) logic, and SET analogues of complementary metal oxide semiconductor (CMOS) logic. SET-based inverter, NAND and NOR logic gates, programmable SET-based logic gates, exclusive-OR (XOR) logic gates, and 'majority logic' gates are discussed. The chapter then considers devices operating using charge state logic. The most widely used scheme is binary decision diagram (BDD) logic, where charge packets are switched through a network formed by two-way switches into one of two output terminals. After an introduction to various BDD gates, the chapter discusses the design, fabrication and characterization of these devices in SOI material, using MTJ few-electron pumps. Finally, the chapter considers 'wireless' logic schemes such as the quantum cellular automaton (QCA) and the single-electron parametron, where arrays of cells formed by quantum dots, switched using electric fields, have been proposed for performing logic operations.

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