

Introduction

Electronic Devices Architectures for the NANO-CMOS Era — From Ultimate CMOS Scaling to Beyond CMOS devices

Since the invention of the first calculation machines, miniaturization has been a constant challenge to increase speed and complexity. Electronic devices have brought, and will bring in the future, a far increasing number of new functions to the basic computing systems such as fast data computing, telecommunication, several kinds of actuations,...which are collectively fabricated on the same physical object named solid state circuit¹, integrated circuit or “chip”. Electronic devices are so small, that billions of basic functions are accessible in a hand held system. Moreover, their unit cost has been divided by more than a factor of 100 millions over the past 30 years! The collective fabrication of electronic devices coupled with the increase of their speed has given a tremendous success, which is unique in the history of mankind, to Micro and Nanoelectronics by continuously introducing innovations in the fabrication process (Fig. 1). Linear scaling of devices dimensions to a quasi-nanometer level allows to build complex systems integrated on a chip (Fig. 1) which reduce drastically their volume and power consumption per function, whilst tremendously increasing their speed. In the future, opportunities will appear to build systems in a molecule. Nanoscience and Nanotechnology researchers join their efforts to Nanoelectronics actors in order to offer mankind possibilities of pervasion of their knowledge into the construction of nanosystems.

Electronic Devices Architectures for the NANO-CMOS Era, is a review for the use of Nanoelectronics, Nanoscience and Nanotechnology researchers and engineers, in which we address:

- (1) the options to linearly scale down logic CMOS or memories;
- (2) the possible competing breakthrough architectures allowing to relax on the linear scaling challenges;
- (3) the new paths for integrated electronics.

The pending alternatives are two ways:

- (1) try to continue the scaling of *Ultimate CMOS* requesting new materials or

(2) introduce new devices, systems architectures or paradigms *Beyond CMOS*. These questions are very much linked to the progress law that microelectronics has been following since the 1960's.²

In the 1960's, Gordon Moore² first reported a progress law of microelectronics by asserting that the number of transistors on a chip will increase by a factor of 2 every year. Electrostatics and power dissipation weighed versus the efficiency/speed of devices, required scaling rules which Robert Dennard, Giorgio Baccarani and co authors^{3,4} expressed in the 1970's and 1980's. Since then, linear scaling of silicon devices has been dominating the microelectronics world due to the success of miniaturization techniques through collective fabrication, even though bipolar transistors have been replaced by CMOS. Today, the most advanced production integrated circuits are built on CMOS devices with minimum feature sizes of 40 nm. Scientists and engineers are facing, for the first time, new challenges dealing with ultimate scaling of CMOS devices. For example, a high dielectric constant (HiK) material is introduced to replace SiO₂, because the scaling

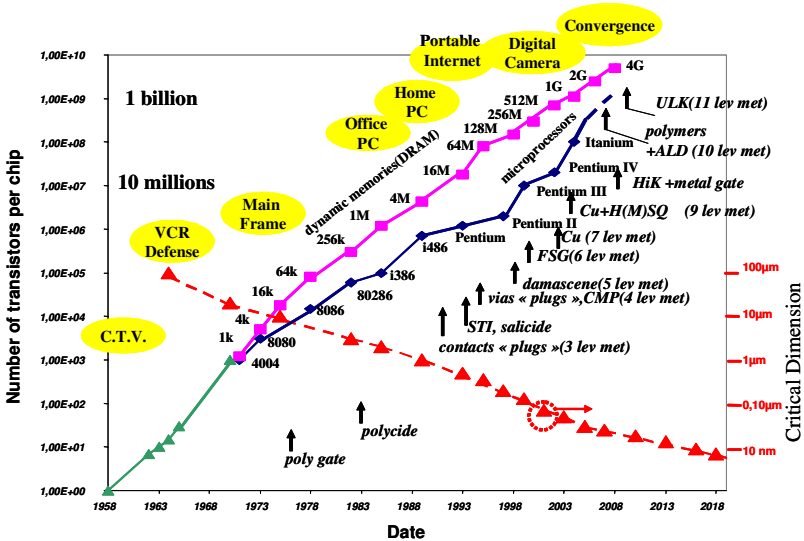


Fig. 1. Evolution of microelectronics devices since the invention of integrated circuits in 1958. On the double Y-axis, the number of transistors per chip (on the left hand side) and their critical dimension (gate length) (right hand side) are reported. Fabrication technology (arrows) and System (bubble) innovations are indicated.

of CMOS gate oxide cannot satisfy anymore the power dissipation specifications required to design practical and usable chips for the increasing Nomadic market needs. Other roadblocks appeared in microelectronics history in the 90's such as the whole interconnect system functionality and density which was enabled by the introduction of the plug concept technology and copper interconnect.

Device physicists and microelectronics engineers have been investigating various paths to continue the integration race through linear scaling down of silicon devices and searching new devices architectures or new state variables and why not new information processing paradigms.

We first overview the possible technological boosters that will allow CMOS nanoelectronics to reach the end of the roadmap in section 1. The challenges for Core CMOS and memory devices architectures scaling are addressed in sub sections 1 and 2. The various architectures and the physics of ultimate MOSFETs require to benchmark integration limits and transport in ultra small devices. These aspects are overlooked in Chapters 1 and 2 by S. Deleonibus *et al.* and T. Poiroux, G. Lecarval respectively. Possible materials alternatives are compared for channel, gate stack and source and drain engineering. What strain can bring to transport properties is reviewed by S. Takagi *et al.* for SOI or GeOI condensed channels in Chapter 3. A major breakthrough that has been expected for more than 10 years has finally been announced for manufacturing of large scale devices: high dielectric constant materials (HiK) are now used as gate dielectrics in combination with metal gates. In Chapter 4, H. Wong *et al.* address the issue of keeping high channel mobility together with low dielectric leakage current. The properties of rare earth oxides, promising for the realization of the HiK and the future scaling, are reviewed and benchmarked. Access resistance becomes a severe issue whenever shallow junctions are scaled down as far as bulk Si or SOI devices are concerned. In Chapter 5, B. Mizuno highlights the promising potential of new doping techniques such as plasma doping combined with laser thermal processing or fast thermal processing to activate the dopants.

In the next decade, active devices architectures will need some breakthroughs whereas interconnect architectures went through the same issues in the 1990s. In Chapter 6, S. Laval *et al.* stress on the eventual use of optical interconnect and interfaces in Nanoelectronics chips to replace Copper. How can this paradigm help in reducing the power consumption and increase speed? After exploiting interchip solutions at the level of a system, intra chip solutions are the major research subjects today.

The challenges for memory devices are numerous. Achieving low writing and access times combined with high retention time is still the Holy Grail searched for high density memory devices. In Chapter 7, K. Kim and G. Jeong review the main challenges in the different served applications to improve memory power consumption, speed and density evolving towards versatile devices properties.

FeRAM and MRAM have been considered as good candidates for fast operation of highly non volatile memory: they are very seductive to microelectronics engineers because these devices can be as fast as DRAM and demonstrate high retention times. In Chapter 8, Y. Arimoto reviews, their potentialities after recalling their principles based on remanent polarization of Ferroelectric insulators capacitors for FeRAMs or magnetic tunnel junctions in MRAMs.

Current flash memories based on floating gate electron charging will be potentially limited by retention issues beyond the 32 nm node, whenever a reduced number of electrons will be used for switching or charge storage operation. In Chapter 9, B. de Salvo and G. Molas review the potentiality of discrete traps storage nodes to recover high retention: Silicon nanocrystals or molecules used in different conformations, or oxido-reduction states in self organized or cross bar matrices are likely to be considered for future high density low cost memories.

If the above mentioned solutions to proceed on the CMOS roadmap are not efficient or fully operating, we will need to consider new paths to propose alternatives or explore new paradigms bringing added value to circuit designs. Section 2 is devoted to the exploration of New Concepts for Nanoelectronics. CMOS operation at nanometer range dimensions or molecules will use a reduced number of electrons. In Chapter 10, J. Gautier *et al.* address the question on the operation of single electron devices based on Coulomb blockade. If these devices cannot replace CMOS straightforwardly, they could be associated in a hybrid architecture for niche type of applications due to their very high charge sensitivity, or offer increased functionalities if an extra control gate is added.

In the nanoscale range, the operation of functions by using molecules is of interest due to their potential compacity. In Chapter 11, D. Vuillaume describes the electronic properties of organic monolayers and molecular devices. Hopefully, tunnel barriers, molecular wires, rectifying and NDR diodes, bistable and memories devices have been demonstrated possible with extension to cross bar architectures of highest density.

Carbon nanotubes (CNTs) have demonstrated very exciting characteristics on the thermal and electrical sides whereas their band structure can allow to build semiconductor or metal based devices. In Chapter 12, V. Derycke *et al.* achieve an overview from the materials electronics properties to the building of field effect transistors (FETs) demonstrating high carrier velocity and long carrier mean free path. The placement of CNTs and sorting their chirality are still issues to solve if one wishes to build circuits.

The ITRS teaches us that it is quite difficult to achieve the lowest power consumption together with high performance with electron charge based devices. Could we transfer state variables other than electron charge to address low power and high performance devices architectures? One of the alternatives could be based on spin transfer and detecting it selectively through so called spin valves. In Chapter 13, Kyung-Jin Lee and Sang Ho Lim give an historical review of spin electronics through the use of magnetoresistance in memory devices to the latest attempts to realize so called spin-FETs.

Searching alternative ways to enhance the efficiency of computing that contribute to the improvement of power/speed systems figures of merit is a permanent challenge for design. Can quantum wave functions be used for computing, allowing thus an infinite number of states per bit and compete with binary type operation based algorithms? In Chapter 14, P. Jorrand addresses the basic principles of quantum information processing and communication. The success of quantum algorithms has been proven in speeding up integer factoring or unordered search.

The authors of this review are well-recognized researchers in their field and have give then best to realize this review of the research on the state of the art of NanoCMOS architectures and beyond. They came from well-recognized universities, institutes and microelectronics companies worldwide to deliver tremendous efforts to develop devices and systems using nanotechnologies that make our daily life objects complex functions possible.

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