

DESIGN CONSIDERATIONS FOR INTEGRATED MODULATOR DRIVERS IN SILICON GERMANIUM TECHNOLOGY

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We present design considerations for high speed high swing differential modulator drivers in SiGe BiCMOS technology. Trade-offs between lumped and distributed designs, and linear and limiting amplifiers are examined. The design of a 6 V output modulator driver is discussed in detail. The driver features a unique bias generation and distribution circuit that enables low power-supply operation. Simulation results and measurements are given.

Keywords: modulator;driver;distributed;amplifier;limiting;bias;SiGe.

1. Introduction

The seemingly insatiable demand for bandwidth has led to the deployment of optical networks operating at several tens of gigabits per second. Commercial time division multiplexed systems (TDM) running at 40 Gbps are now a reality.^{1 2 3} The block diagram of a typical OC-768 transceiver is shown in Figure 1. Four 10 Gbps datastreams are multiplexed together. This stream, with a data rate of 40 Gbps, is amplified and drives a Mach-Zehnder interferometric optical modulator. The optical modulator needs to be driven with a large differential waveform.

At the receiver, a photodiode is used to convert the optical signal into an electrical one. The photodiode current is amplified by a transimpedance amplifier (TIA) and further processed by a limiting amplifier, which converts the small signal TIA output to a large two-level signal. This in turn drives the clock and data recovery unit (CDR), and a demultiplexer that splits the 40 Gbps stream into four 10 Gbps datastreams. While much of the electronics in earlier generation OC-768 transponders was designed in compound semiconductor technologies,^{4 5 6} it has now become feasible to realize most of the functionality in silicon germanium (SiGe) BiCMOS processes. SiGe provides an opportunity for unparalleled system integration, as high

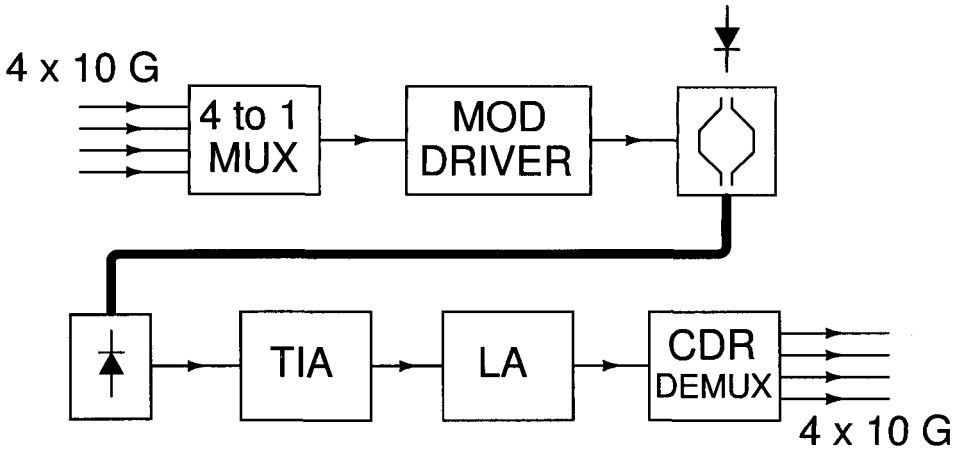


Fig. 1. Block diagram of an OC-768 transceiver.

performance bipolar transistors and CMOS devices can be included on the same chip. Many of the building blocks for OC-768 transceivers, like multiplexers and demultiplexers (MUX/DEMUX), transimpedance amplifiers (TIA), limiting amplifiers (LA) and clock and data recovery units (CDR) have been reported in SiGe BiCMOS processes.^{2 3} These are testimony to the maturity and reliability of state of the art SiGe processes.

The design of the modulator driver presents some unique challenges due to the high speeds and high voltage swings involved.^{8 9 10} A typical value for the common-emitter breakdown voltage, $BV_{CE,O}$ in these technologies is about 1.8 V. Other major challenges are electro-migration in the interconnect metalization, and the formation of hot-spots due to oxide isolation of the bipolar transistors. Hot-spots could degrade device performance due to self-heating. In order to reduce the power dissipation of the driver, it is necessary to keep the power supply as small as possible. In this work, we present the design of a modulator driver with a fully differential output swing of 6 V peak-to-peak swing, implemented in a SiGe process, with nominal supply voltage of 6 V. Designed for operation at OC-768 data rates, the driver features a unique bias distribution technique. The rest of this paper is organized as follows. In Section 2, we compare the merits of a lumped versus distributed driver design and present the evolution of the gaincell used in the design. In Section 3 we show the chip architecture and discuss circuit details. We present in detail the development of the tail current bias control technique in Section 4. We show simulations and experimental results in Sections 5 and 6 respectively. Conclusions are given in Section 7.

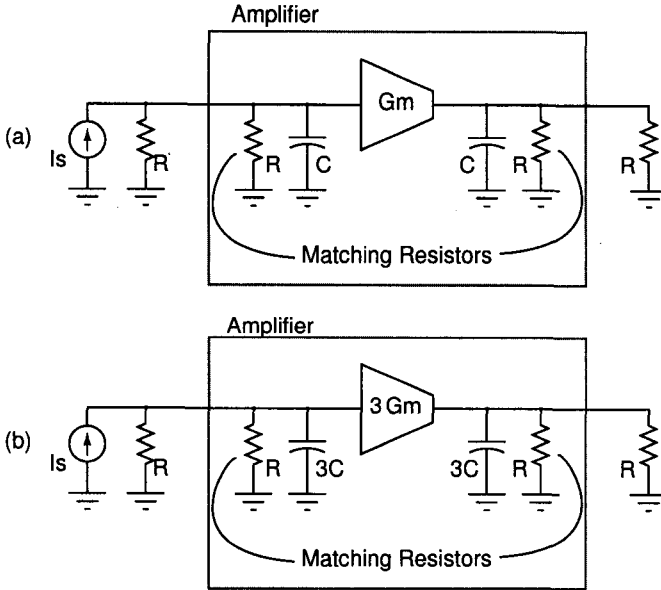


Fig. 2. Gain bandwidth limitations of lumped amplifiers.

2. Driver Architecture

2.1. Lumped versus Distributed Design

Consider the design of an amplifier using a transconductor (G_m) with input and output capacitors of value C , as shown in Figure 2(a). The source and load impedances are resistors of value R . At low frequencies, the input and output impedances of the amplifier are matched to the source and load respectively. The input and output capacitances and the resistors form poles that result in a finite bandwidth, which is inversely proportional to RC . The low frequency gain is proportional to $G_m R$, so the gain-bandwidth product of the amplifier is proportional to G_m/C .

In order to obtain a higher DC gain (e.g. $3G_m R$), the transconductance has to be increased by a factor of three, as shown in Figure 2(b). This increase in gain is accompanied by a proportional decrease in bandwidth due to the three-fold increase in input and output parasitic capacitances. Hence, the gain-bandwidth product remains the same as in the low-gain case. A technique to increase the gain-bandwidth product is distributed amplification, where the input and output capacitances of the active device are "absorbed" into a synthetic transmission line, as shown in Figure 3. The characteristic impedance of this line is $Z_o = \sqrt{L/C}$. Thus, L must be chosen to be equal to $R^2 C$. For a thorough exposition of distributed amplifiers, the reader is referred to Wong's book¹¹. It can be shown that a distributed amplifier trades off bandwidth for latency, and the performance depends critically on the

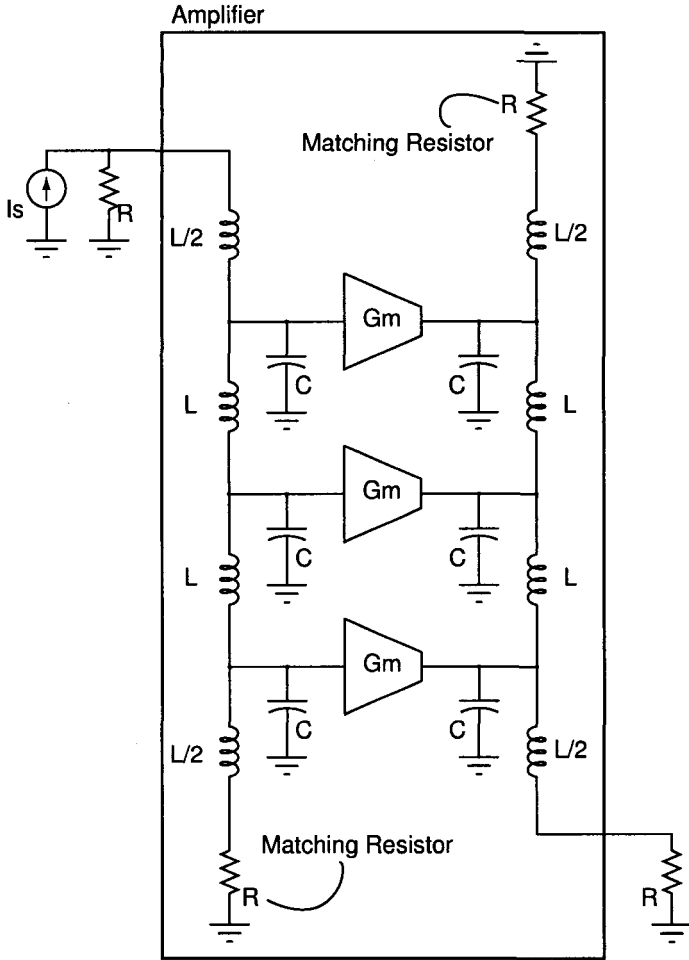


Fig. 3. The distributed amplifier with lumped elements.

delay synchronization between the input and output transmission lines. While the amplifier in Figure 3 uses lumped inductors for broad banding, the same effect can be achieved with transmission lines, as shown in Figure 4. τ represents the time of flight of the transmission lines. Noticing that a transmission line section can be approximated as shown toward the right of the figure, we see that the value of Z_1 and τ need to satisfy

$$R = \sqrt{\frac{Z_1 \tau}{\frac{\tau}{Z_1} + C}} \tag{1}$$

Given Z_1 , R and C , the delay of the transmission line required can be calculated

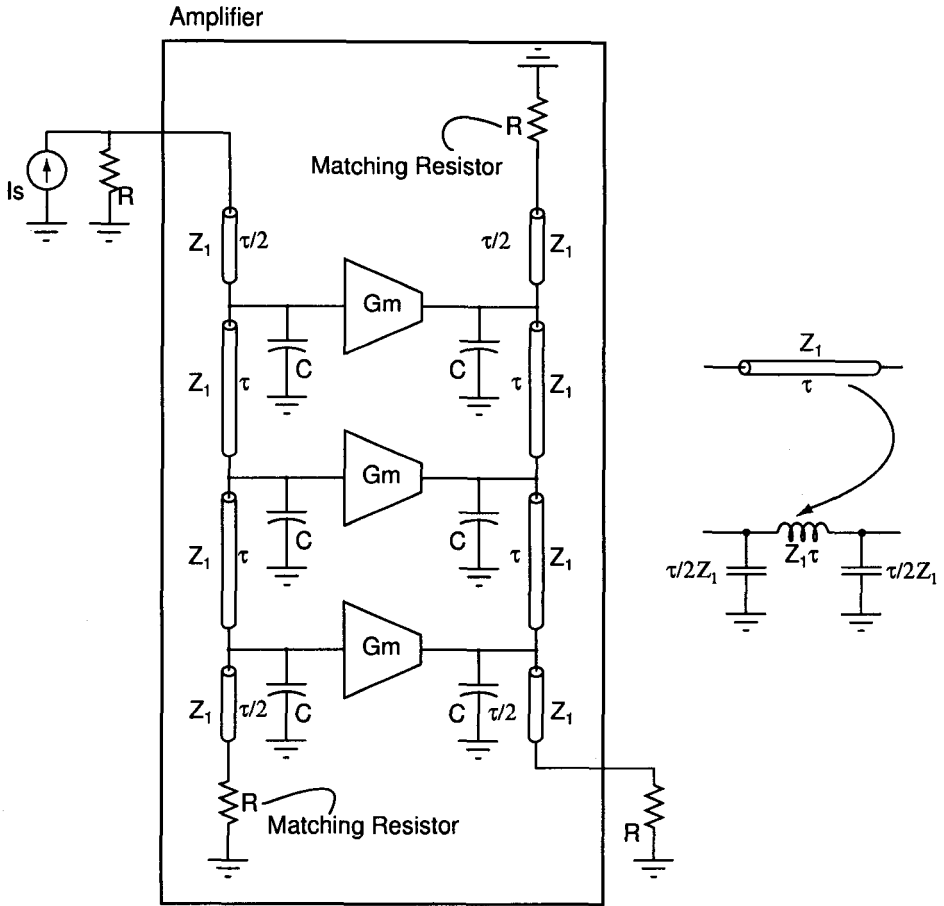


Fig. 4. The distributed amplifier with transmission line broadbanding.

to be

$$\tau = CR \frac{Z_1/R}{(Z_1/R)^2 - 1} \quad (2)$$

A microstrip line was chosen as the transmission line structure in our chip. The characteristic impedance of a microstrip line decreases with increasing width, so from the discussion above, we would like to make the line narrow. In this application, however, the output lines are required to carry large amounts of current, which necessitates a wide line. Hence, large voltage swings and high bandwidth have inherently contradictory requirements.

In our design the input capacitance of the “transconductors” was about 30 fF. A characteristic impedance of about 65Ω was chosen for Z_1 as a compromise between chip dimensions and electromigration in the output transmission lines.

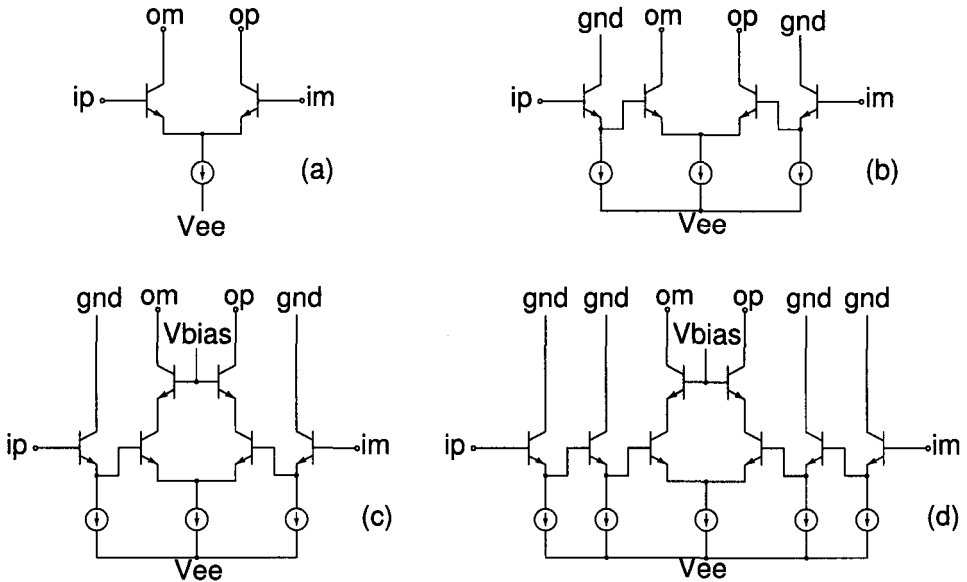


Fig. 5. Evolution of the gaincell.

2.2. Linear versus Limiting Gaincell

Another key design decision that needs to be made is regarding the input-output behavior of the gaincell - should this be linear, or could it be a limiting type of design ? It turns out that the answer to this question depends on the application. This design being intended for NRZ data, linearity is not required. Moreover, a linear gaincell would consume a lot more power than a limiting one because only a small portion of the quiescent current would be modulated by the input signal. Since power dissipation of the entire driver is of significant concern, a limiting gaincell is one of choice here.

2.3. Fully Differential Gain Cell Design

Figure 5 shows the evolution of the gaincell. The very basic current switch that come to mind is shown as (a) in the figure. Here the tail current is switched between op and om depending on the sign of the input differential voltage. It is being easy to layout, but the input and output capacitances are vastly different. Moreover, the input capacitance is lossy. These reasons make it difficult to synchronize the delays of the input and output lines of the traveling wave structure. The overlap capacitances between input and output nodes also cause problems.

The structure of Figure 5(b) uses emitter-followers to drive the input of the current-switching pair. This bring the input and output capacitances closer, but still suffers from the problems caused by input-output overlap capacitances of the

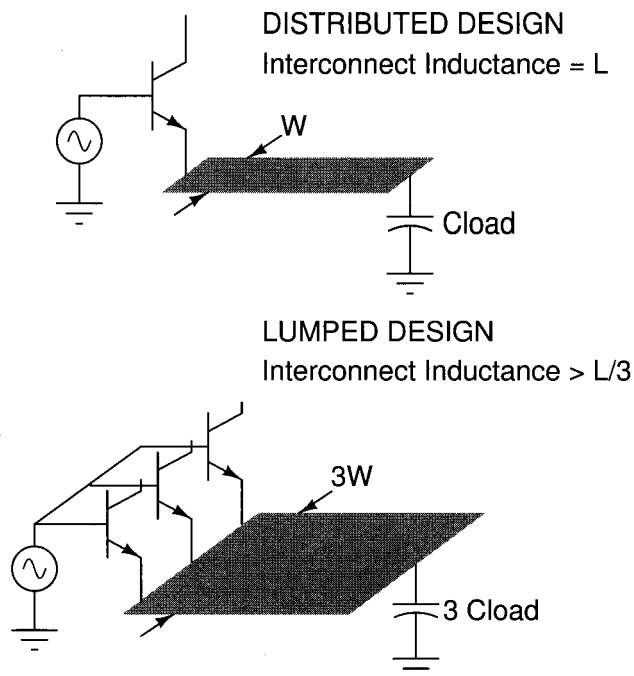


Fig. 6. Lumped versus distributed gaincells with interconnect inductance.

switch.

Input-output isolation is improved by using a common-base stage at the output of the current switch as shown in Figure 5(c). We found that another buffer stage was required to make the input and output capacitances of the gaincell equal. The final topology of the gaincell is shown in Figure 5(d).

It is apt to mention at this juncture some additional benefits that accrue from the distributed nature of the driver. Notice that the gaincell has several emitter followers driving successive stages, that typically present a capacitive load. Due to the large bias currents involved in the design, the impedance levels of operation are extremely low (few ohms). This means that inductance of the interconnect can severely degrade the performance of the circuit. Consider the case of an emitter follower driving a capacitive load in a 3 stage distributed amplifier, as shown in Figure 6. The width of the wire connecting the emitter to the capacitive load is denoted by W , while its series inductance is denoted by L . Assume that the design is stable. Consider now a lumped version, shown toward the lower part of the figure. It has to drive thrice the load capacitance with one-third the source impedance. It would be just as stable as the distributed amplifier if the interconnect inductance scaled to $L/3$. However, the inductance is much higher than $L/3$ (even though the wire width is $3W$) due to mutual coupling effects. Hence, the stability of the lumped

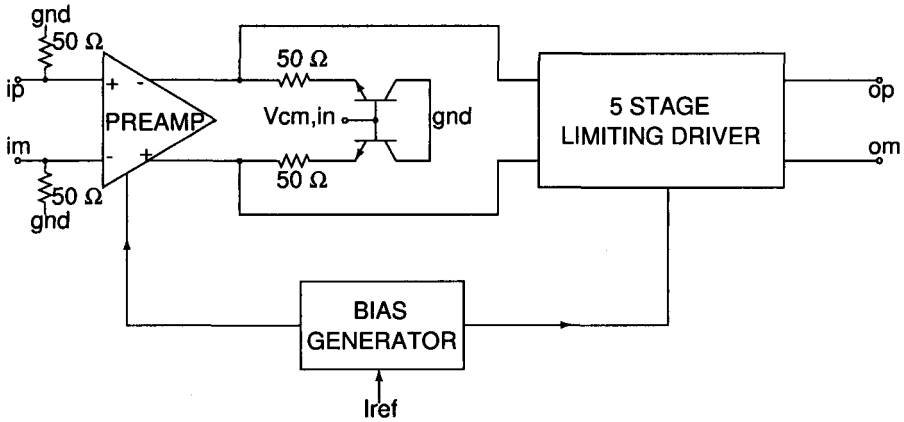


Fig. 7. Modulator driver chip architecture.

version is degraded.

Another aspect where a distributed design wins over a lumped one is that of thermal hot-spots. In a lumped design all the power is dissipated in one area, potentially heating up local interconnect and reducing long term reliability. On the other hand, a distributed design has many smaller sources of heat, distributed over the chip, which is thermally a more favored situation.

3. Circuit Details

The architecture of the entire chip is shown in Figure 7. It consists of a preamplifier driving a five stage distributed limiting amplifier. The preamplifier (shown in Figure 8) takes in an external input and generates a fully differential 600 mV_{pp} drive at a correct common-mode voltage suitable for the main driver. The first emitter follower level shifts the input common mode, while the second is used to drive the current switch.

For the driver, a five stage design represented a reasonable trade-off between the cut-off frequency of the artificial transmission input and output transmission lines on one hand and complexity involved in biasing multiple gaincells on the other. The power supply voltage was chosen to be $V_{ee} = -6\text{ V}$.

The schematic of the gaincell used in the main amplifier is shown in Figure 9. The emitter followers were biased with resistors and diodes. Their collectors are connected to a voltage lower than ground, to prevent breakdown of the devices. The tail current source of the current switching pair is biased with a MOSFET in order to save headroom. The low output resistance of the MOSFET, combined with the desired stability of the driver peak-to-peak output swing necessitates very careful biasing of the tail current source. This is discussed in detail in the next section.

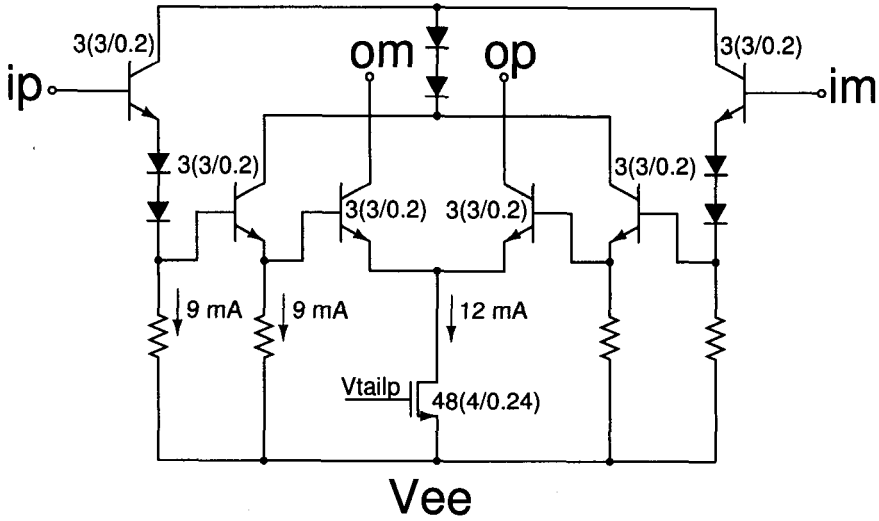


Fig. 8. Schematic of the preamplifier.

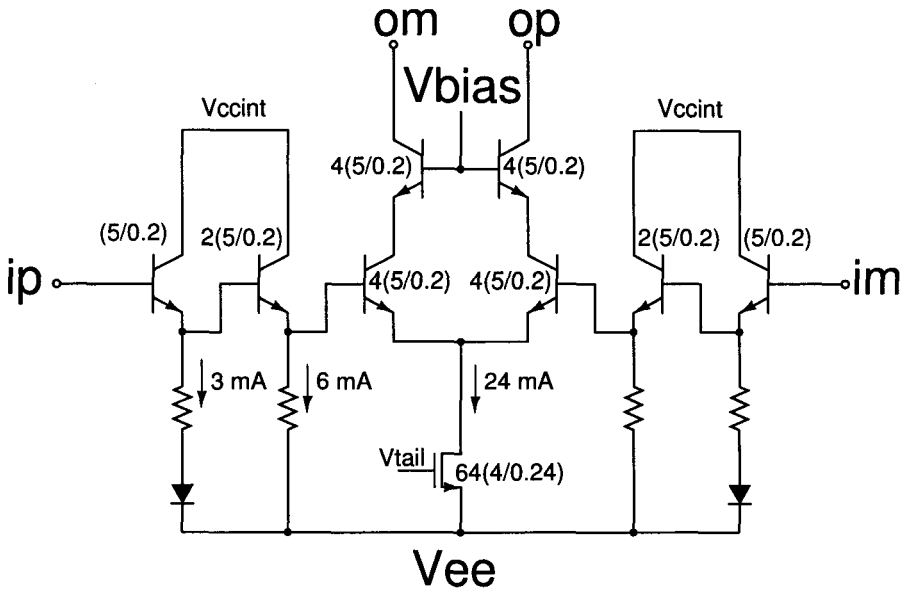


Fig. 9. Schematic of final gaincell used in the main amplifier.

4. Tail Current Bias Generation & Distribution

In this section, we discuss the important issue of accurately generating the required tail current for the current switching pair. Since the driver is a limiting distributed

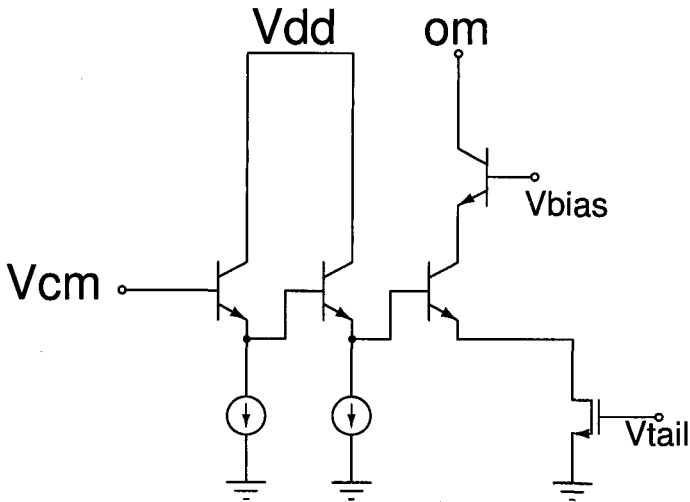
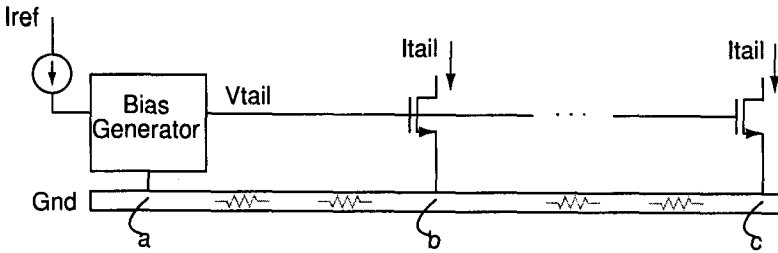
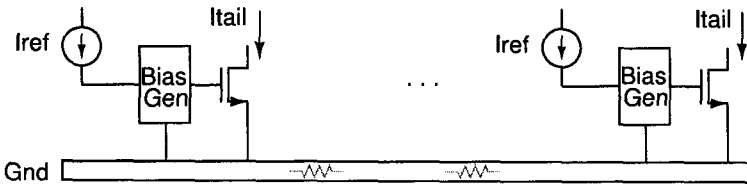


Fig. 10. Half circuit of the gaincell.

amplifier design, the peak-to-peak output swing is directly proportional to the tail current - so this current must be constant across power supply voltage, process variations and temperature. Further, as we wish to minimize the power supply voltage required for the driver IC, a MOS transistor is a more appropriate choice for realizing the current source. The half-circuit of the gaincell incorporating a MOS tail current source is shown in Figure 10.

We are faced with two basic choices for generating and distributing V_{tail} .

- **Global V_{tail} generation :** Here the required bias voltage is generated at one point on the chip and distributed to all transistors that require it, as shown in Figure 11. This approach has the advantage that very little extra power is required by the bias generator. However, there are several serious drawbacks associated with this scheme. Due to the distributed topology and high currents involved in the design there could be significant voltage drops along the ground bus (i.e, points a,b,c are not at the same potential). This means that the actual gate-source voltages appearing across M1-M5 could be very different from what was intended. Any threshold voltage mismatch between the devices used in the bias generation block and the actual current source transistors would also lead to tail currents that were poorly controlled over process and temperature variations. Hence, global generation of V_{tail} is not a viable approach.
- **Local V_{tail} generation :** In this approach, a bias generator is placed in proximity to each gain cell, as shown in Figure 12. The reference current I_{ref} has to now be distributed to each gaincell, so the total power dissipation in the bias section increases. However, since the bias generator is placed


 Fig. 11. Global V_{tail} generation & distribution.

 Fig. 12. Local V_{tail} generation.

close to the gaincell, ground drops between gaincells is of no consequence. Further, this technique only demands MOS transistor threshold voltage matching within a gaincell, in contrast to a global V_{tail} generator, where matching must be maintained across great distances on the die. Hence, the local bias generation approach is used in this work.

We now present the operating principle of a precision bias circuit used in this work. The schematic is shown in Figure 13, where the gaincell is shown towards the right. $M1'$, $D1$, $D2$ and $Q3'$ in the bias generation network are sized so that they have the same current density as $M1$, $Q1$, $Q2$ and $Q3$ respectively. A current I_{ref} is forced into the collector of $Q3'$ and the negative feedback loop formed through $Q6$, $D5$, $D4$ and $M2'$ determines V_{tail} . Note that $M1'$ and $M1$ operate with identical terminal voltages regardless of process variations or temperature, so that in the absence of mismatch, the tail current is determined given by $I_{tail} = n I_{ref}$. C_c is the compensating capacitor for the bias negative feedback loop. The DC β 's of the bipolar transistors in SiGe are very high (several hundreds), so there is negligible error due to the base current of $Q6$.

While this replica feedback bias generator is very precise, it is complicated to lay out. Note that V_{cm} and I_{ref} lines need to be propagated to all the gaincells. With this, there also exists the possibility of parasitic coupling between gaincells through the V_{cm} bias line. The capacitor C_c is of the order of several picofarads, and is therefore unwieldy to place in the gain cell. As far as ease of layout is concerned, the most desirable circuit is shown toward the right of Figure 14. Here, only one

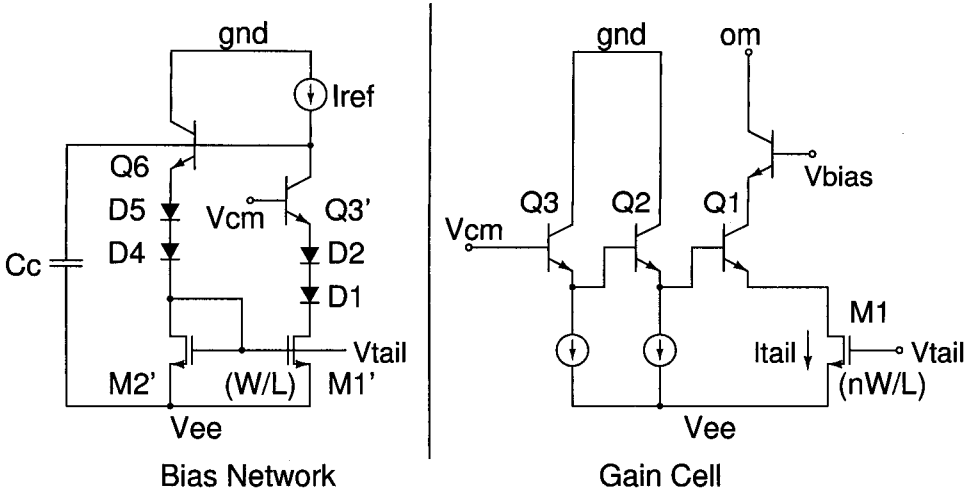


Fig. 13. Precision bias voltage generation using replica feedback.

line (I_{ref}) goes to every cell, and no compensation capacitor is needed. However, it has the disadvantage that the tail current in the gaincell is not precisely set due to the difference in drain-source voltage of the FETs in the bias generator and the gaincell. The tail current can be shown to be

$$I_{tail} = n I_{ref} \frac{1 + \lambda V_{DS,M1}}{1 + \lambda V_{DS,M1'}} \tag{3}$$

where λ is the channel length modulation parameter of the MOSFETs. I_{tail} is not precise since λ , $V_{DS,M1}$ and $V_{DS,M1'}$ vary with process and temperature.

An improved bias circuit which combines the advantages of both techniques discussed above is possible. The kernel of the idea is the following - if the reference current to the layout friendly circuit is precompensated for the difference in V_{DS} of the FETs in the bias generator and the tail current source, then good precision can be obtained. The implementation of this principle is shown in Figure 15. I_p , the predistorted current in $M2'$ is seen to be

$$I_p = I_{ref} \frac{1 + \lambda V_{DS,M2'}}{1 + \lambda V_{DS,M1a'}} \tag{4}$$

Hence the tail current is given by

$$I_{tail} = n I_{ref} \frac{1 + \lambda V_{DS,M2'}}{1 + \lambda V_{DS,M1a'}} \frac{1 + \lambda V_{DS,M1}}{1 + \lambda V_{DS,M2a'}} \tag{5}$$

Since $V_{DS,M2'} = V_{DS,M2a'}$ and $V_{DS,M1a'} = V_{DS,M1}$, we see that $I_{tail} = n I_{ref}$ and is independent of process and temperature. The predistortion block is common to all

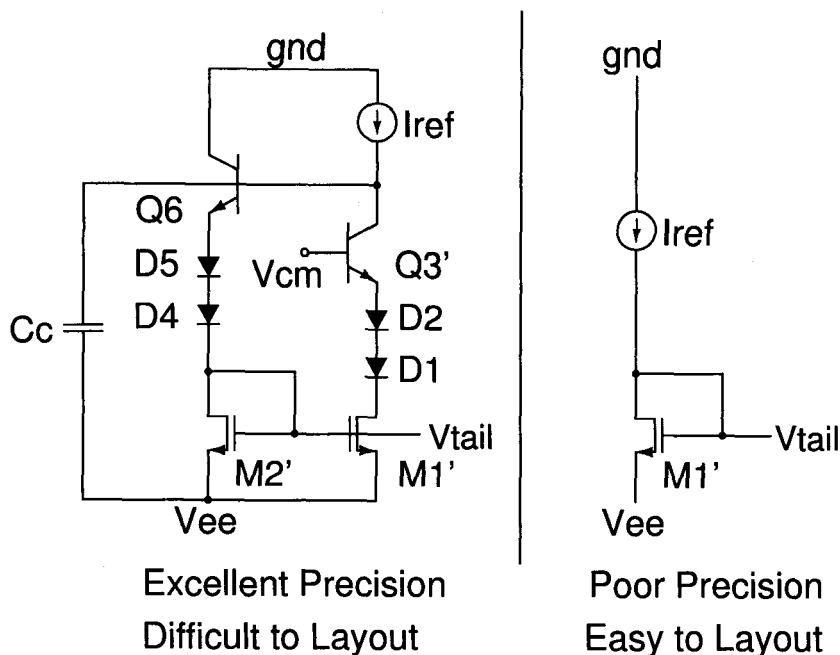


Fig. 14. Comparison of two bias generation techniques.

the gaincells and is placed at one corner of the chip. The predistorted currents are propagated to the gain cells. Layout is straightforward as the bias generator is a simple structure. Since currents are distributed, there is no problem with regard to drops along the ground lines as explained earlier in this section.

5. Simulated Performance

In this section, we present simulated results for the modulator driver IC. Figure 16 shows the drive voltages at the inputs of the gaincells of the main amplifier. Notice that the peak-to-peak differential drive voltage is 600 mV (which is the output drive of the preamplifier) and the delay in the drives to successive stages is about 3.2 picoseconds. Figure 17 shows the driver output with an input step. It shows a 6 V peak-to-peak differential output voltage with a 10-90% risetime of 10.8 ps. Figure 18 shows the simulated eye-diagram. A summary of these simulated performance is shown in Table 1.

6. Experimental Results

In this section we present measurement results from a modulator driver fabricated in a $0.18\ \mu\text{m}$ SiGe BiCMOS technology. The chip micro photograph is shown in Figure 19. The chip area is about $1.5\ \text{mm}^2$. Figure 20 shows the eye-diagram of the

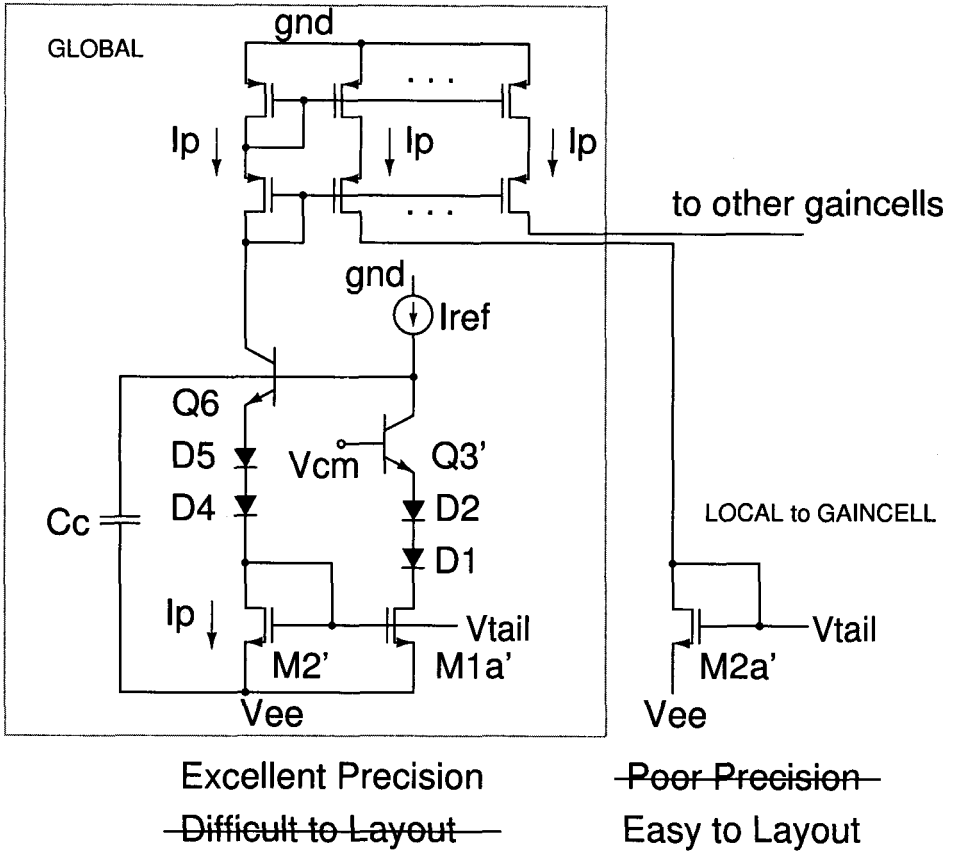


Fig. 15. Precision bias technique with simplified layout.

Table 1. Summary of simulated characteristics (25°C)

Technology	0.18 μm SiGe BiCMOS
Supply voltage	-6.0 V
Output Voltage Swing	6 V (peak-to-peak differential)
Input Voltage Drive	400-600 mV (peak-to-peak differential)
Rise Time (20-80%)	6.7 ps
Rise Time (10-90%)	10.8 ps
Chip area	1.5 mm ²
Current Drain from Vee	\approx 300 mA
DC gain	20 dB

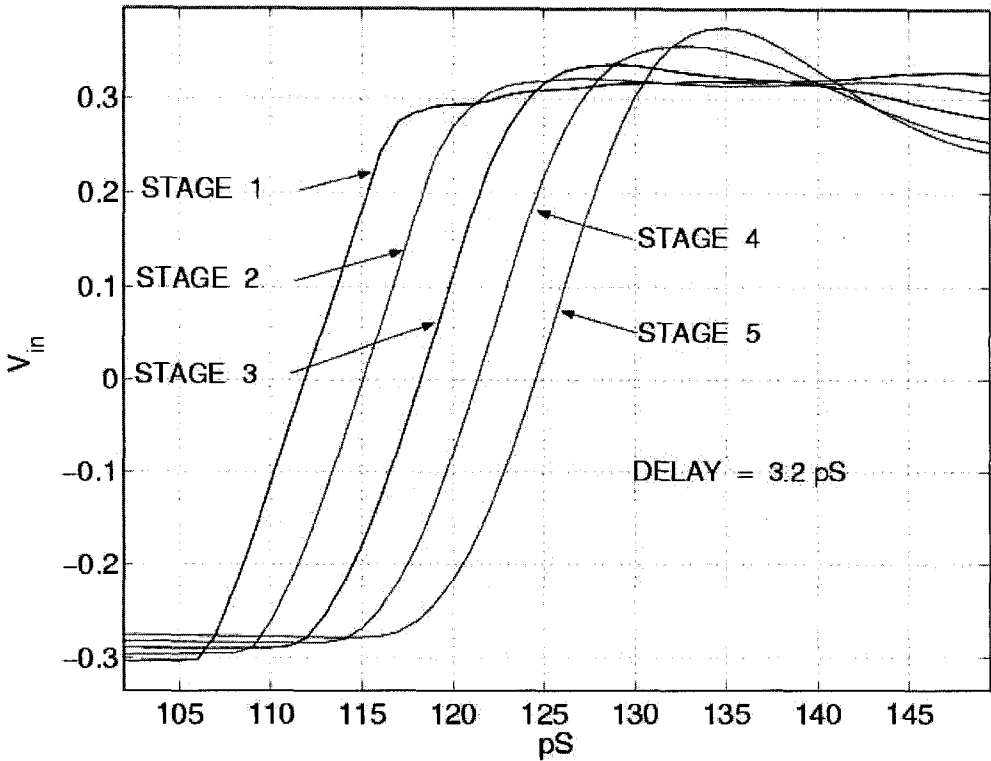


Fig. 16. Inputs to the successive gaincells of the modulator driver.

driver at a data rate of 12.5 Gbps. The input was provided by an Anritsu MP1758A pulse-pattern generator. The output eyes were recorded with an Agilent 86100A DCA using the Agilent 83484A 50GHz plug-in module. A 16dB attenuator was used on the output of the modulator driver before measuring it on the DCA. The 12.5 GHz clock output of the pattern generator was used to trigger the DCA. To generate a 40 Gbps stream four 10 Gbps streams from the Anritsu pulse generator were multiplexed using an in-house 4-to-1 mux. The resulting single-ended driver output eye is shown in Figure 21. Eye closure is attributed to the test setup and the quality of the input eye to the driver.

7. Conclusions

Design considerations for high-speed high swing modulator drivers in SiGe technology were presented. A novel technique for generating and distributing bias voltages was discussed. Simulation and experimental results for a 6 V_{pp} differential modulator driver designed in a 0.18 μm technology were given.

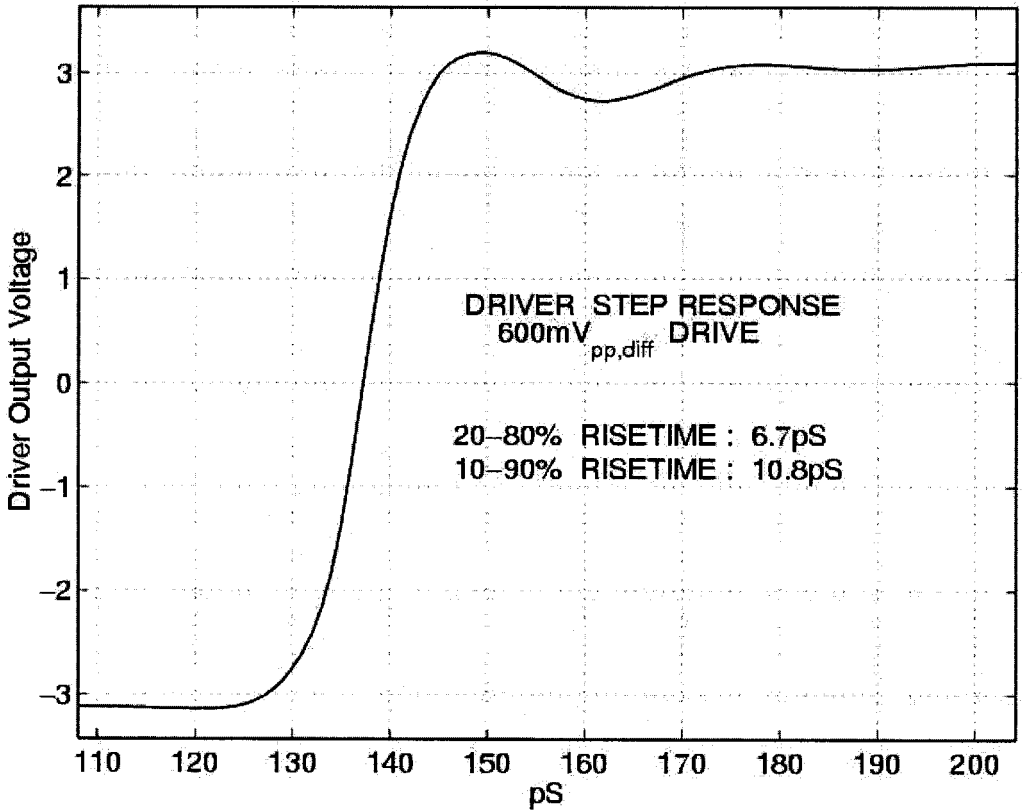


Fig. 17. Differential output step response of the driver.

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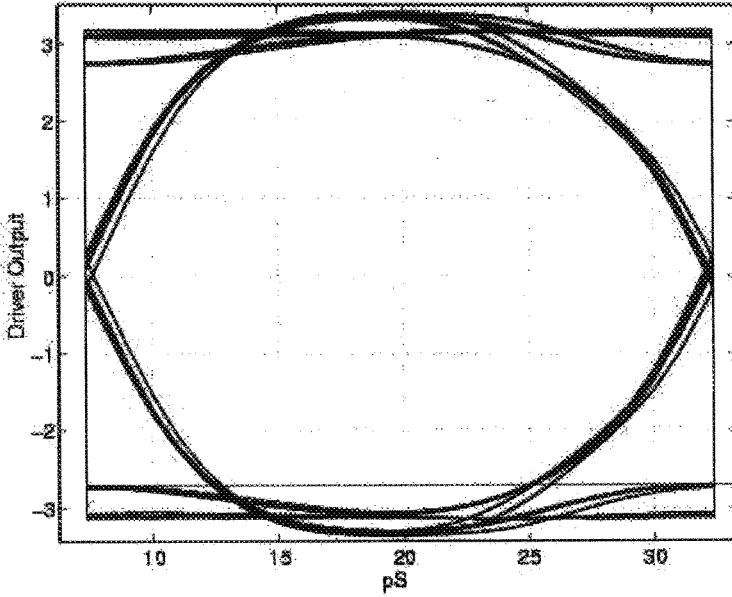


Fig. 18. Simulated eye diagram at the driver output at 40 Gbps.

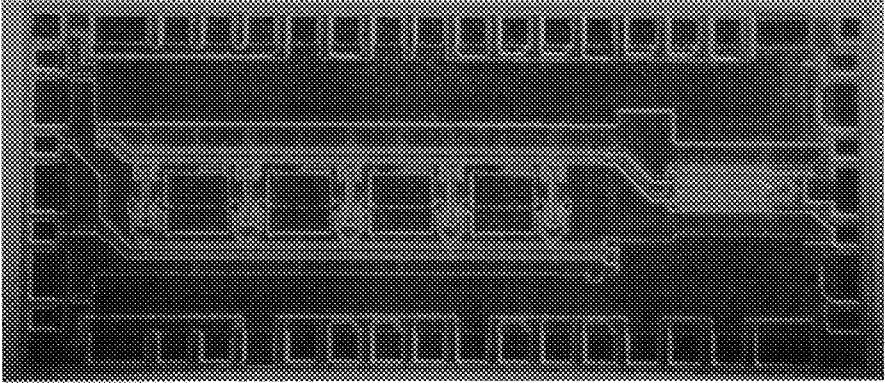


Fig. 19. Microphotograph of the chip.

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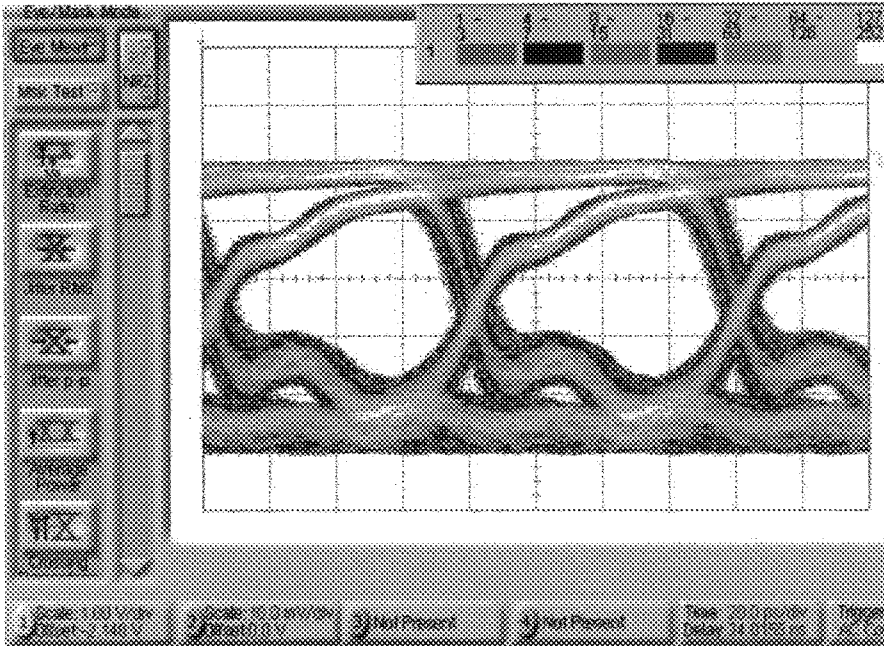


Fig. 20. Driver output eye-diagram for 12.5 Gbps data.

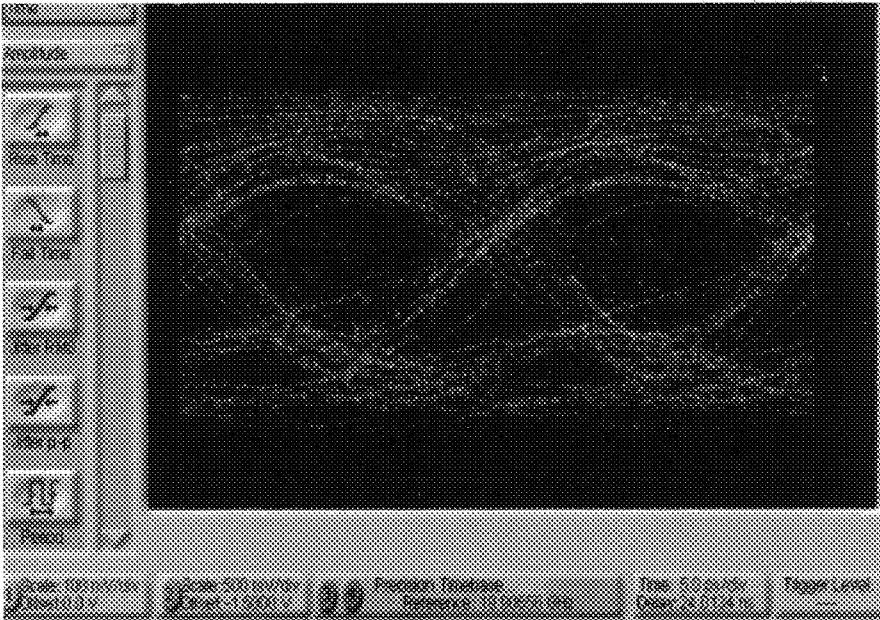


Fig. 21. Driver output eye-diagram for 40 Gbps data.

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